

## HAMILTON and AREA PACKET NETWORK.

The first meeting, an organizational and technical one, was held at the Canada Centre for Inland Waters seminar room on Sunday, January 25 at 14:00. 15 people attended and we found a lot of interest in the network among them.

This, then, is the result of that meeting! the first in a series (hopefully) of bulletins of the newly formed, nebulous group henceforth to be known as the Hamilton and Area Packet Network.

In response to requests at the meeting and our own ideas and input, this bulletin contains something for everyone.

A brief summary and minutes of the meeting is given. You will also find an introduction to SDLC protocol from 'Technical Aspects of Data Communication' by John E. McNamara. This is the protocol generated and interpreted by the Intel 8273 chip on the VADCG board.

For the person interested in entering the network, the question 'What do I need to get going?' is answered.

In the circuits department, you will find how I connected into the sequel circuitry of my Heath HW-202, a circuit of the modem designed by Bill Montgomerie based on the Exar application note AP-01, and the circuit of my initial station node card, currently in use as a terminal node controller in my S-100 system using modified LIP and TIP software. You will also see how to add LED indicators to the VADCG board, and some hints on getting the board running.

In the software department, Robert Sleath's TIP using the 8255 parallel chip and interface is given. His keyboard and VRAM appear as 8-bit devices. His TIP also includes a mini monitor, entered by CTRL-R and allowing the user to load locations in RAM, dump any location in both ASCII and hex, and to jump to any location. You will also find Bill's down line loader as adapted by Stu, and a down-loadable routine to test the added LED indicators. The modification to the LIP by Stu to move RST vectors to RAM is listed, as is the portion of the LIP used to issue commands to the 8273.

Our initial mailing list is included, followed by the Exar application note and spec sheets on the 2206 and 2211.

Last, but not least is the initial Packet Radio Bibliography.

The next meeting will be called in about a month (late Feb or Mar) by phone and announcement on 146.46 and 145.65 MHz.

Things to look forward to in the next bulletin are John's (MUV) Trap dump routine and other interface schematics from Max, Glenn and John. We also hope to discuss applications.

## HAMILTON and AREA PACKET NETWORK

2391 Arnold Crescent,  
Burlington, Ontario,  
L7P 4J2, Canada.

What do I need to get going?

To begin at the beginning...

- 1) a real interest in contributing to the development of the network, either by getting involved with the implementation, or creating or making use of applications for the other users.
  - 2) a 2 metre rig with either 146.46 or 145.65 (or both)
- This much will get you in touch with what is going on currently.

- 3) a Bell 202 modem, suitably augmented, or a simple 202 compatible one, such as that in the circuits department. Set up to run at 1200 baud using 1200 Hz and 2200 Hz tones. cost to build - \$50 or less depending on ingenuity. (Power can be taken from VADCG ps and TTL levels can be used to connect to VADCG)
  - 4) a VADCG card (\$32) plus parts. VADCG no longer puts kits together, so chips might run \$250 or more. There are some SDLC chips available for about \$45 (Cdn) see Stu.
  - 5) a power supply to run the VADCG board and modem. About \$40 or less (depending, again, on ingenuity)
  - 6) a terminal type device: teletype, glass or otherwise, or some form of computer to emulate one. (information is available on CP/M programs for terminal emulation. APPLE and TRS-80 have similar routines, I am sure.
  - 7) custom programming for your TIP. People are available who can burn 2708 EPROMs for you.
- And that's about it.  
Except for an amateur license of course (wish me luck with the code!!!).
- A digital license is not required since the mode in use is F2 (AFSK), and when we move to 220, just plain FSK.

MAKE GOOD THINGS HAPPEN.

ALL DONATIONS CHEERFULLY ACCEPTED!

The two flags which delineate the SDLC frame serve as reference points for the position of the address and control fields and initiate the transmission error checking. The ending flag indicates to the receiving station that the 16 bits just received constitute the Frame Check. The ending frame could be followed by another frame, another flag, or an idle. Note that this means that when two frames follow each other, the intervening flag is simultaneously the ending flag of the first frame and the beginning flag of the next frame. Since the SDLC protocol does not use characters of defined length, but rather works on a bit by bit basis, the 01111110 flag may be recognized at any time.

In order that the flag not be sent accidentally, SDLC procedures require that a binary 0 be inserted by the transmitter after any succession of five continuous 1s. The receiver then removes a 0 that follows a received succession of five 1s. Inserted and removed zeros are not included in the transmission error check.

The address field is eight bits long and designates the number of the secondary station to which the command from the primary station is being sent. The control field is an additional eight bits and can have three formats: "information transfer format," "supervisory format," and "nonsequenced format." The only thing in common between the three formats is the P/F (poll/final) bit. A frame with the P(poll) bit set is sent from a primary station to a secondary station to authorize transmission, and a frame with the F(final) bit set is sent by the secondary station in response to the poll. Typically, the primary station will send a number of frames to a particular secondary station, each frame having the P/F bit a 0, until the primary station is finished and ready for the secondary station to respond. At this time the primary station will send a frame having the P/F bit set to 1. The secondary station will recognize that the primary station desires a response and will reply, perhaps with a number of frames, each having the P/F bit a 0. Then, when the secondary station is completing its response to the "poll," it will send a "final" frame which has the P/F bit set to 1.

The three control formats are summarized in Table 19-1.

## CHAPTER 19 SDLC AND BIT ORIENTED PROTOCOLS

It is not the intent of this chapter to be a definitive source on SDLC, but rather to describe enough of its operation for the reader to get the general idea and to be able to more readily understand more detailed references on the subject.

First, a few definitions should be given. Any data communication link involves at least two participating stations. The station which has responsibility for the data link and which issues the commands to control that link is called the "primary station." The other station is a "secondary station." It is not necessary that all information transfers be initiated by a primary station. Using SDLC procedures, a secondary station may be the initiator.

The basic format for SDLC is a "frame," shown in Figure 19-1. The information field is not restricted in format or content and can be of

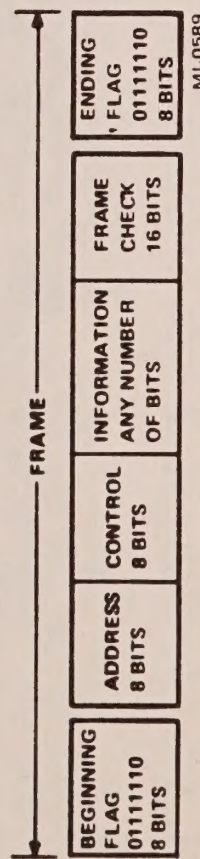


Figure 19-1. Basic SDLC Frame

any reasonable length (including zero). The maximum length is that which can be expected to arrive at the receiver error-free most of the time, and is hence a function of communication channel error rate.

Table 19-1. SDLC Control Field Formats

Format	Bits				Acronym
Information	Nr	P/F	Ns	0	1
Supervisory	Nr	P/F	00	01	RR
	Nr	P/F	01	01	RNR
	Nr	P/F	10	01	REJ
Nonsequenced	000	P/F	00	11	NSI
	000	F	01	11	RQI
	000	P	01	11	SIM
	100	P	00	11	SNRM
	000	F	11	11	ROL
	010	P	00	11	DISC
	011	F	00	11	NSA
	100	F	01	11	CMDR
	001	1	00	11	ORP
<div>Sent Last →</div> <div>→ Sent First</div>					

The information format is used for ordinary data transmission and is the only one of the three formats that uses frame sequence numbering. Each frame transmitted in this format is numbered so that the receiving station can tell if any are missing; when retransmission is required, the receiving station can tell the transmitting station which frame to start with in the retransmission. A station that transmits sequenced frames counts and numbers each frame. This count is known as Ns. A station receiving sequenced frames counts each error-free sequenced frame that it receives; the receiver count is called Nr. The Nr count advances when a frame is checked and found to be error-free; Nr thus becomes the count of the "next expected" frame and should agree with the next incoming Ns count. Returning to the format shown in Table 19-1, the initial 0 bit indicates that this control field is in information format, the three Ns bits are "this is the message number I am sending," the P/F bit is set if the station is concluding its poll or its response to a poll, and the three Nr bits are "this is the message number I am expecting next."

The supervisory format is used in conjunction with the information format to initiate and control information transfer in the information format. The first two bits sent, 1 and 0, designate that this control field is in supervisory format. The next two bits indicate which command this is: RR, RNR, or REJ. An RR (Receive Ready) can be sent by either a primary or a secondary station, and indicates that all sequenced frames up through Nr-1 have been received correctly, and that the originating station is ready to receive some more. RNR (Receive Not Ready) can also be sent by either a primary or a secondary station, and also acknowledges messages up to Nr-1. Unlike RR, however, RNR indicates a temporary busy condition in which no additional frames that require buffer space can be accepted. REJ (Reject) is a command/response which may be transmitted to request transmission or retransmission. It acknowledges successful receipt of frames up through Nr-1 and requests Nr and following frames.

The nonsequenced format is used for setting operating modes, initializing stations, etc. As the name implies, nonsequenced communications are not sequence checked and do not use the Nr and Ns system. The first two bits sent, 11, indicate a nonsequenced format, the P/F bit has its usual meaning, and the remaining five bits in the control field are used for encoding the various commands and responses.

The commands and responses encoded in the nonsequenced format control field are listed below.

**NSI (Nonsequenced Information):** This indicates that the information which follows in the variable length information field is being sent separately from any sequenced message presently in progress.

**RQI (Request for Initialization):** This is transmitted by a secondary station when it wishes the primary station to send an SIM command. If the primary station sends something other than SIM, the secondary station sends another RQI.

**SIM (Set Initialization Mode):** This command initiates system-specified procedures at the receiving secondary station for the purposes of initializing. Nr and Ns counts are set to 0 at both the primary and secondary stations. The expected response to SIM is NSA.

ignored and the transmitter sends the complement of the resulting remainder value, with the high order bit first.

One other feature which should be discussed is the procedure for prematurely terminating a data link. This is called "abort" and is accomplished by the transmitting station's sending eight consecutive 1 bits. The abort pattern may be followed by a minimum of seven additional 1s to idle the data link, or it may be followed by a flag. The purpose of a flag following an abort is to clear the CRC function at the receiver.

The preceding has been a rather condensed description of SDLC and the reader is advised to read IBM's "IBM Synchronous Data Link Control — General Information" (GA27-3093 File GENL-09) for further information. The reader is also referred to documentation on ADCCP and HDLC for a look at some similar protocols.

DONATIONS TO HELP WITH  
PUBLICATION COSTS AND  
POSTAGE CHARGES  
ACCEPTED

COMING:-

DIGITAL COMMUNICATION 2  
MODULATION BIBLIOGRAPHY

MORE THAN 200 REFERENCES  
FROM THE LITERATURE AND  
GOVERNMENT CONTRACT REPORTS.

**SNRM (Set Normal Response Mode):** This command subordinates the receiving secondary station to the transmitting primary station, and the secondary station is not expected to initiate any transmissions unless requested to do so by the primary station. The Nr and Ns counts at both the primary and the secondary stations are reset to 0. The secondary station remains in this mode until it receives a DISC or SIM. The expected response to SNRM is NSA.

**ROL (Request On-Line):** This is transmitted by a secondary station to indicate that it is disconnected.

**DISC (Disconnect):** This command places the secondary station effectively offline. That station cannot receive or transmit information frames and remains disconnected until it receives an SNRM or SIM command. The expected response to DISC is NSA.

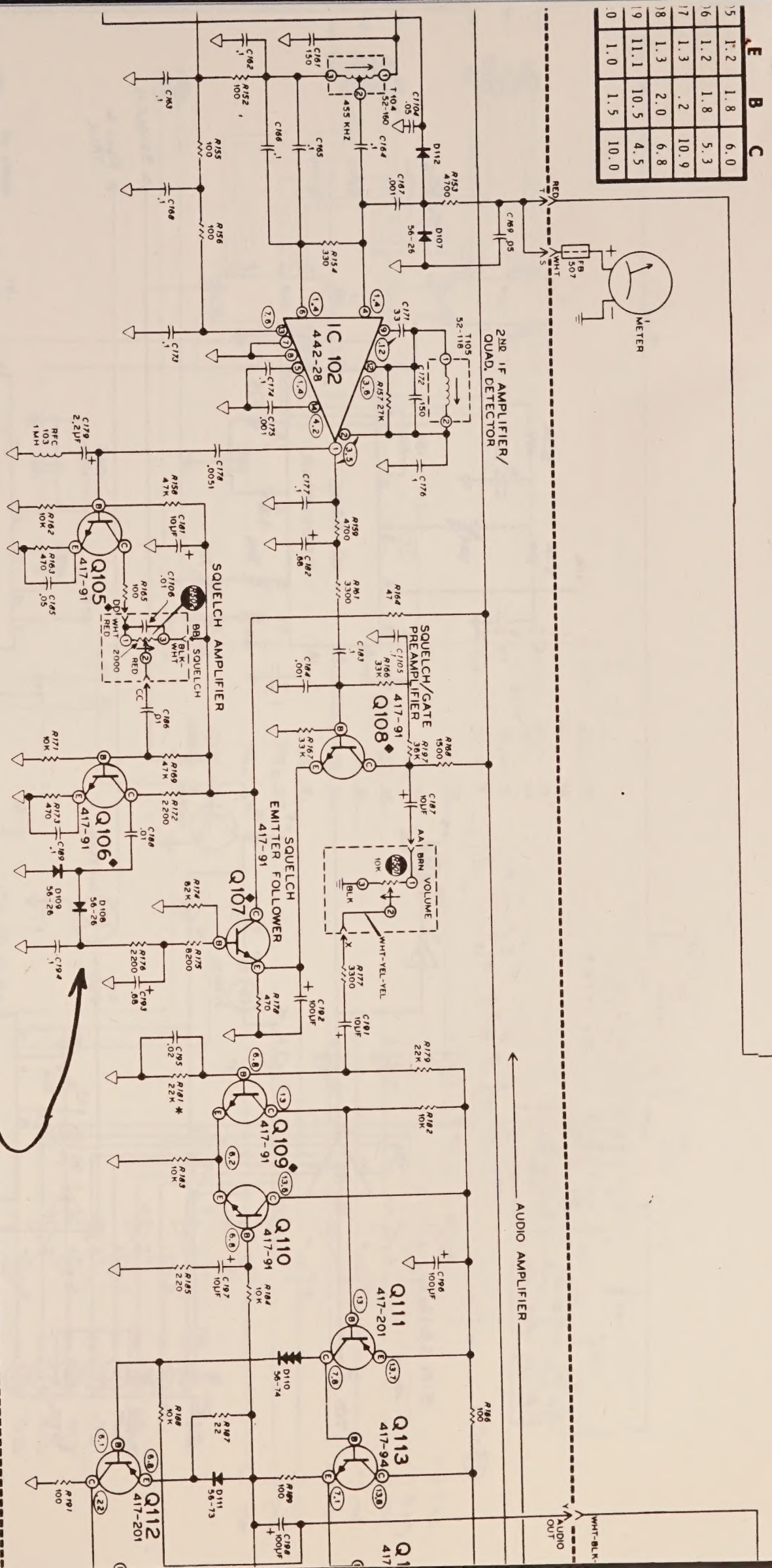
**NSA (Nonsequenced Acknowledgement):** This is the affirmative response to SNRM, DISC, or SIM.

**CMDR (Command Reject):** This is the response transmitted by a secondary station in normal response mode when it receives a non-valid command. A frame with CMDR in the control field has an information field following which is arranged in a fixed format which reports that station's present Ns, that station's present Nr, and four bits which indicate 1) an invalid or non-implemented command, 2) an information field associated with a command which isn't supposed to have one, 3) an information field that was so long it caused buffer overrun, or 4) the Nr received from the primary station does not make sense, given the Ns that was sent to it.

**ORP (Optional Response Poll):** This command invites transmission from the addressed secondary stations.

While SDLC is simpler in most aspects than previously discussed protocols, the block check calculations are a good deal more complex. The first difference is that the transmitting station begins with a "remainder value" of all 1s rather than the customary all 0s. The binary value of the transmission is premultiplied by  $X^{16}$  and divided by the generating polynomial  $X^{16} + X^{12} + X^5 + 1$ . The quotient digits are

	E	B	C
5	1.2	1.8	6.0
6	1.2	1.8	5.3
7	1.3	.2	10.9
8	1.3	2.0	6.8
9	11.1	10.5	4.5
0	1.0	1.5	10.0



HEATHKIT

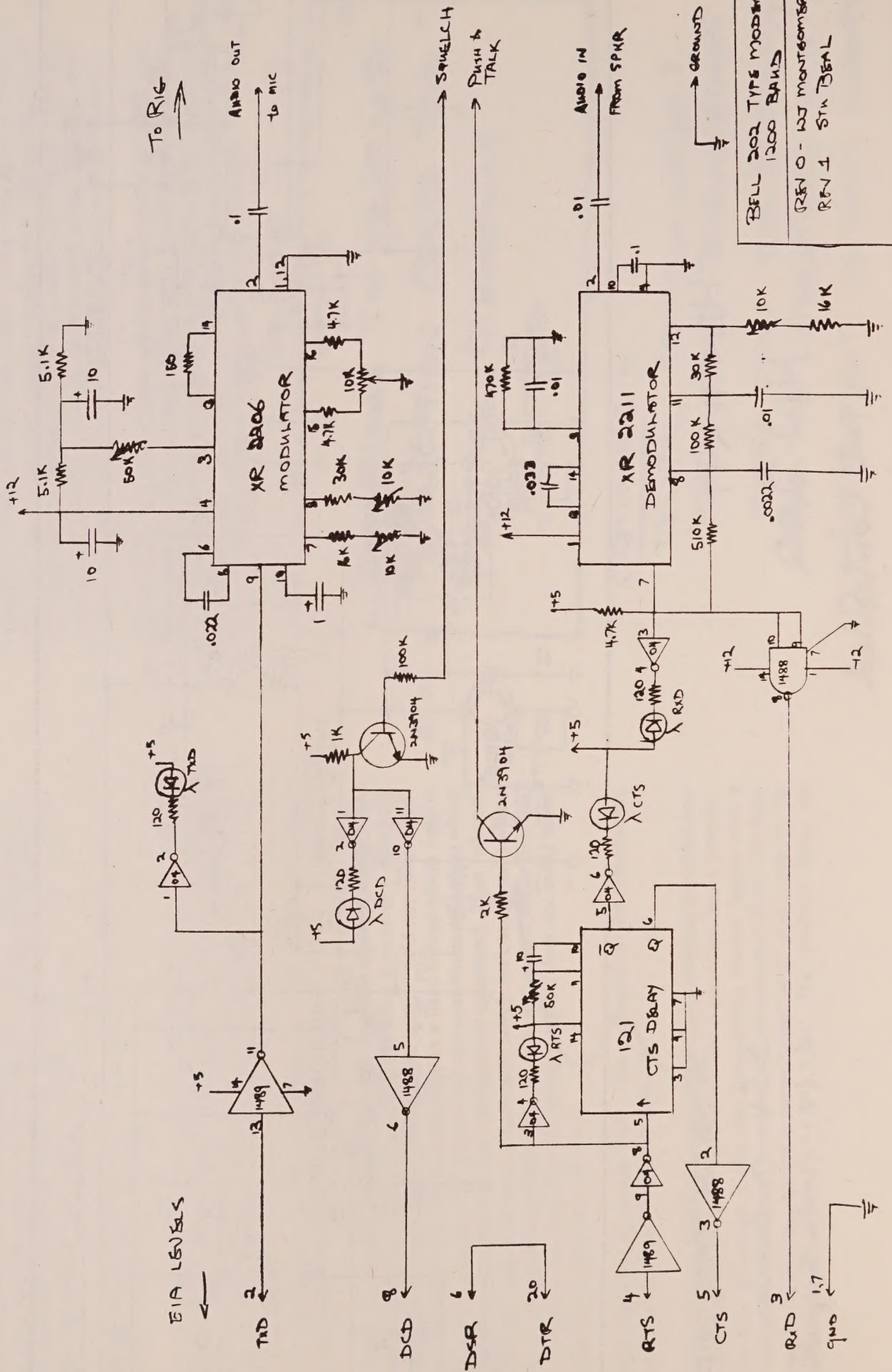
HW 202

XTR controlled.

SQUELCH TAKE OFF

$\approx 5V$  no carrier  
 $< 1V$  with signal

3797





#### Additional LED indicators on the VADCG board.

In case you are going to do some of your own software development for the VADCG board, here is the way I hooked up some LED indicators to give me some re-assurance that the software was operating and certain conditions were present (or absent).

There are 4 lines available for setting under program control.

They are:

- 1) SOD on the 8085 processor (use RIM and SIM to alter)
- 2) -OUT2 on the 8250 UART (I/O to UART command register)
- 3) -PB3 on the 8273 (point F on the board)
- 4) -PB4 on 8273 (point G- for both use I/O to command reg.)

I connected these 4 locations to the inputs of 7406 open collector inverters and pulled up the collector thru a 120 ohm resistor and a LED:



The only problem is that SOD has a positive true state while the others are negative true. Thus the software SETs SOD to turn the LED OFF and CLEARs it to turn ON. The other bits work correctly.

The code used to operate the LEDs is found in the Down Line Loader module, listed in the software section. The location referred to as CMDOUT is the same CMDOUT in the LIP; the routine used to setup the 8273.

Also included in the software section is a test routine which, when down loaded, flashes the 4 LEDs in 1,2,3,4,1,2,... sequence.

To re-car: the LEDs are connected to SOD (pin 4) on the 8085, -OUT2 (pin 31) on the 8250, -PB3 (pin 38) and -PB4 (pin 39) on the 8273.

The code for operating the SOD LED should be modified to preserve the interrupt status by doing a RIM, the SOD masking and setting and then a SIM, rather than just a SIM.

#### Down Line Loader for the VADCG board.

Some work was done by both John Vanden Berg (NUV) and Bill Montgomery (EC) to fiddle with the board using programs loaded down line to it from a host processor.

Stu Real modified the initialization portion of the LIP to cause the RST vector table to be moved into RAM at RESET time.

Thus a combination of these allows the user to down load modules and intercept the vectoring for interrupts, etc. and process them himself.

Bill's adapted Down Line Loader and Stu's LIP modifications are listed in the software section.

Entry to the loader is by TRAP interrupt. (The board needs to have one trace cut to allow the TRAP operation. It isn't difficult to find the place; see schematic)

The loader accepts INTEL HEX format ASCII and loads it at the designated locations. The single character '\*' following loading transfers directly to address 01000 Hex (start of real RAM).

John uses the TRAP interrupt (suitably de-bounced) to cause a register save and memory dump operation for debugging.

#### Bibliography.

The first copy is being distributed to the people who attended the meeting on Sunday, January 25. Because of the size of the item, we are forced to charge about \$5.00 for additional copies. A second bibliography on modulation techniques will be available shortly. Details will follow.

The Packet bibliography contains over 200 references to the literature and to reports of U.S. government contracts. Generally the citations include the publisher and catalog number if appropriate.

Unfortunately because two searches were done some months apart (by computer, of course) there may be some duplicate citations but not many; the first search ended early in 79 and the second was limited to 79 and 80.

Also, because of the strategy used for searching some (perhaps) unwanted papers were cited; i.e. because I wanted (DIGITAL COMMUNICATION) & (RADIO or WIRELESS) several papers on Infrared (wireless) communication fell out.

The exact strategy was:

[ (PACKET or NETWORK or PROTOCOL or ALOHA) and  
(COMPUTER\* or COMMUNIC\*) ] and  
(RADIO or WIRELESS)

The following is a summary of the indicated interests in the proposed network: i.e. the things people would like to be able to do on the net, in order of popularity:

file transfer	12
message centre	10
packet video	9
games and simulation	7
on line bulletin composition	7
interactive graphics	7
RTTY replacement (HF gateway)	6
on-line swap shop classifieds	6
packet voice	6
remote system use	5
VE7, VE2 gateways	5
CRRS	4

Other interests listed in the Etc. column:  
 Promote low cost entry into Packet Radio  
 Standardization on State-of-the-Art Hardware and protocols

# Hints on setting the VANDG board up and running.

Once built, examine for all mechanical defects (shorts, cold solder) then apply power. WITHOUT chips on the board. Verify there is the correct voltage at all pins of the sockets (4-5, 4-12, open, ground).

Turn power OFF!

Insert 8085 and XTAL and divider chip (CMOS- careful).

Power up and attempt to see clock transitions at 1/2 clock out from 8085, and lower frequencies on the divider.

If no clock or if frequency seems strange, put 20pf from each side of XTAL to ground. (Seems to help startup on-frequency)

Power off.

Insert remainder of chips, including PROMS with LIP and TLP.

Power on (SMOKE TEST).

Examine the Tx data line of the 8273 for flags (continuous transitions) the DTR line (-PR2) should go to -12 while reset held down (+4 if only TTL outputs, not RS-232) and should go to +12 (0 if TTL) soon after button released.

MACRO-80 3.36

17-Mar-80

PAGE 1

## **DLTTEST**

INCLUDE 8250.HEF  
 C 9250 SERIAL I/O ENVARIES  
 C .LIST

04EB

CMOUT

EDU

04EBH

FLASH:

MVI

SIH

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

OUT

CALL

ORI

SIH

CALL

MVI

TIP Ba R. SLEATH (V836FED)

CP/M MACRO ASSEN 2.0 #001 VARIOUS TERMINAL MODE COMMUNICATIONS PROGRAM - MODULE TIP-11

```
*****
; ** VARIOUS TERMINAL MODE COMMUNICATIONS PROGRAM - MODULE TIP-11
; ** BY DOUG LOCKHART, VETAPU MAY, 1980
; **
; LAST CHANGED: BY R. SLEATH 20 NOV 90
; TERMINAL INTERFACE PROGRAM
; THIS PROGRAM IS WRITTEN TO RUN IN THE VARIOUS TERMINAL MODE CONTROLLER. IT
; INTERFACES WITH A MODE COMMUNICATIONS PROGRAM RUNNING AT ADDRESS 0 IN
; MEMORY. THIS VERSION IS WRITTEN TO USE THE 8255 PROGRAMMABLE I/O PORT
; TO COMMUNICATE WITH A LOCAL TERMINAL.
```

MACLIB LIB85

```
INCRB MACRO
    MVI A,1
    RST 2
    ENDM

INCLB MACRO
    MVI A,2
    RST 3
    ENDM
```

```
; RAM CONSTANT - CHANGE FOR DIFFERENT RAM LOCATION
LORAM EQU 1000H ; START OF RAM STORAGE
```

```
; NON-ZERO STATUS MEANS LINE BUFFER ADDRESS IS IN HL REG.
; ZERO STATUS MEANS NO BUFFER IS READY
NEXTIN MACRO
    RST 4
    ENDM
```

; 8255 PARALLEL I/O EQUATES

```
0008 = PORTA EQU 8 ; PORT A INPUT AND OUTPUT
0009 = PORTB EQU 9 ; PORT B INPUT AND OUTPUT
000A = PORTC EQU 0AH ; PORT C INPUT AND OUTPUT
000B = CONTROL EQU 0BH ; CONTROL PORT OUTPUT ONLY
```

0017 = RIM EQU 17H ; REQUEST INITIALIZATION MODE CONTROL BYTE

0008 = MSE EQU 08H ; MASK SET ENABLE BIT

PAGE

; COMMON COMMUNICATIONS AREA

; CIRCULAR TERMINAL BUFFER VARIABLES

1000 = CCA EQU LORAM ; ADDRESS OF BEGINNING OF COMMON COMMUNICATIONS AREA  
1004 = CCB EQU CCA+4 ; CURRENT TERMINAL BUFFER INPUT ENTRY  
1006 = CCA+6 EQU CCA+6 ; OLDEST TERMINAL BUFFER ENTRY  
1008 = CCA+8 EQU CCA+8 ; TERMINAL BUFFER INPUT POINTER  
100A = CCA+0AH EQU CCA+0AH ; TERMINAL BUFFER OUTPUT POINTER  
100C = CCA+0CH EQU CCA+0CH ; LAST TERMINAL BUFFER OUTPUT ENTRY  
100E = CCA+0EH EQU CCA+0EH ; CURRENT TERMINAL BUFFER OUTPUT ENTRY

; CIRCULAR LINE BUFFER VARIABLES

1012 = LBPE EQU CCA+12H ; LINE BUFFER PROCESSING ENTRY  
1014 = CLBE EQU CCA+14H ; CURRENT LINE BUFFER ENTRY ADDRESS  
1016 = OLBE EQU CCA+16H ; OLDEST LINE BUFFER ENTRY  
1018 = LBIP EQU CCA+18H ; LINE BUFFER INPUT POINTER  
101A = LBOP EQU CCA+1AH ; LINE BUFFER OUTPUT POINTER

; MISCELLANEOUS

1000 = STAT1 EQU CCA ; MAINLINE STATUS BYTE  
1003 = TROFLO EQU CCA+3 ; TERMINAL BUFFER OVERFLOW STATUS  
101C = BUFCOUNT EQU CCA+1CH ; CURRENT INPUT BUFFER COUNT  
101D = OUTCOUNT EQU CCA+1DH ; CURRENT BUFFER OUTPUT BYTES REMAINING  
000D = CR EQU 0DH ; ASCII CARRIAGE RETURN  
000A = LF EQU 0AH ; ASCII LINE FEED

PAGE

0800 08G 800H ; WHERE THIS PROGRAM'S FROM STARTS

; ENTRY JUMP TABLE

0800 C31508 JMF TIPINIT ; INITIALIZATION ENTRY POINT CALLED BY  
0803 C32E08 JMF RST55 ; INTERRUPT FROM RST55  
0806 C30608 JMP ; UNUSED INTERRUPT ENTRY POINT  
0809 C3CC08 JMP DISPATCH ; TO DISPATCHER ROUTINE  
080C 0C17564533R1808 DB 12,R18D,'VCESEFD' ; CONNECTION BUFFER  
0814 08 TERMO DB 8 ; THIS NODES TERMINAL NUMBER

TIPINIT:

0815+20 R1M ; UNMASK INTERRUPTS FROM SERIAL INTERFA  
DB ; GET CURRENT INTERRUPT MASK IN A  
0816 E606 ANI 00000110B ; RESET RST5.5 MASK BIT  
0818 F608 ORI MSE ; SET MASK SET ENABLE BIT  
STM ; ENABLE RST5.5 INTERRUPTS  
DB 30H

0818 3E8F MOV A,89H  
081D D308 OUT 08H  
081F AF XRA A  
0820 D308 OUT 08H  
0822 3D DCR A  
0823 D308 OUT 08H  
0825 CDF008 CALL CLEAR  
0828 21E709 LXI H,MESG1  
082B C3DD09 JMP MESOUT

; RETURN TO LIP FOR COMPLETION OF INITIALIZATION

PAGE

082E F5 RST55: PUSH PSW  
082F E5 PUSH H  
0830 05 PUSH D  
0831 C5 PUSH B  
0832 D80A FXINT: IN 0AH  
0834 E67F ANI 7FH  
0836 FE01 CFI 01H  
0838 C24A08 JNZ RXCONT  
083B CDF008 CALL CLEAR  
083E C1A009 CALL UPSCRN  
0841 C3B508 JMP EXIT  
0844 FE02 JZ 02H  
0846 CA7E0A JZ M1M1M  
0849 3A0310 LDA TROFLO  
084C B7 ORA A  
084D C2B508 JNZ EXIT  
0850 2A0610 LHD DTRE  
0853 E8 XCHG  
0854 2A0810 LHD TBIP  
INCRB  
MOV A,1  
RST 2  
JZ FULL  
SHLD TBIP  
IN 0AH  
ANI 7FH  
MOV M,A  
LXI H,BUF-COUNT  
INR H

0857+3E01 0859+D7 085A CAC408 085D 220810 0860 D80A 0862 E67F 0864 77 0865 211C10 0868 34  
; ECHO DATA TO TERMINAL  
MOV C,A ; SAVE DATA BYTE  
TESTCON:  
CFI 1BH ; CONTROL X  
JNZ TESTDIS  
MOV A,0 ; 0 FOR CONNECT  
RST 6  
JMP EXIT  
TESTDIS:  
CFI 19H ; CONTROL Y  
JNZ TXWAIT  
MOV A,1 ; 1 FOR DISCONNECT  
RST 6  
JMP EXIT  
TXWAIT: MOV A,C  
CALL ZCHOUT  
MOV A,C  
LEF  
CFI EXIT  
JNZ EXIT  
MOV A,7CH  
CALL ZCHOUT  
MOV A,M  
MOV M,0  
LHD DTRE  
MOV M,A  
LHD TBIP

086A FE18 086C C27508 086F 3E00 0871 F7 0872 C3B508 0875 FE19 0877 C2B008 087A 3E01 087C F7 087D C3B508 0880 79 0881 C01709 0884 79 0885 FE0A 0887 C2B508 088A 3E9C 088C C01709 088F 7E 0890 3600 0892 2A0410 0895 77 0896 2A0810  
; ECHO DATA TO TERMINAL  
MOV C,A ; SAVE DATA BYTE  
TESTCON:  
CFI 1BH ; CONTROL X  
JNZ TESTDIS  
MOV A,0 ; 0 FOR CONNECT  
RST 6  
JMP EXIT  
TESTDIS:  
CFI 19H ; CONTROL Y  
JNZ TXWAIT  
MOV A,1 ; 1 FOR DISCONNECT  
RST 6  
JMP EXIT  
TXWAIT: MOV A,C  
CALL ZCHOUT  
MOV A,C  
LEF  
CFI EXIT  
JNZ EXIT  
MOV A,7CH  
CALL ZCHOUT  
MOV A,M  
MOV M,0  
LHD DTRE  
MOV M,A  
LHD TBIP

089A FE18 089C C27508 089F 3E00 08A1 F7 08A2 C3B508 08A5 FE19 08A7 C2B008 08AA 3E01 08AC F7 08AD C3B508 08B0 79 08B1 C01709 08B4 79 08B5 FE0A 08B7 C2B508 08BA 3E9C 08BC C01709 08BF 7E 08C0 3600 08C2 2A0410 08C5 77 08C6 2A0810  
; ECHO DATA TO TERMINAL  
MOV C,A ; SAVE DATA BYTE  
TESTCON:  
CFI 1BH ; CONTROL X  
JNZ TESTDIS  
MOV A,0 ; 0 FOR CONNECT  
RST 6  
JMP EXIT  
TESTDIS:  
CFI 19H ; CONTROL Y  
JNZ TXWAIT  
MOV A,1 ; 1 FOR DISCONNECT  
RST 6  
JMP EXIT  
TXWAIT: MOV A,C  
CALL ZCHOUT  
MOV A,C  
LEF  
CFI EXIT  
JNZ EXIT  
MOV A,7CH  
CALL ZCHOUT  
MOV A,M  
MOV M,0  
LHD DTRE  
MOV M,A  
LHD TBIP

089A FE01 089B+D7 089C 220410 089F C2A708 08A2 3E9F 08A4 D70310  
INCRB  
MOV A,1  
RST 2  
SHLD TBIP  
JNZ EXIT  
MOV A,0FFH  
STA TROFLO  
XRA A  
OUT 08H  
DCR A  
OUT 08H  
CALL UPSCRN  
POP B  
POP D  
POP H  
POP PSW  
RET

08A7+3E01 08A9+D7 08AA 220810 08AD C2B508 08B0 3E9F 08B2 320310 08B5 AF 08B6 D308 08B8 3D 08B9 D308 08BB FB 08BC C1A009 08BF C1 08C0 D1 08C1 E1 08C2 F1 08C3 C9  
EXIT:  
XRA A  
OUT 08H  
DCR A  
OUT 08H  
CALL UPSCRN  
POP B  
POP D  
POP H  
POP PSW  
RET

08C4 3E9F 08C6 320310 08C9 C3B508  
FULL:  
MOV A,0FFH  
STA TROFLO  
JMP EXIT  
DISPATCH:  
NEXTIN  
RST 4  
RZ  
MOV A,M  
STA OUT-COUNT  
INCRB 3  
MOV A,3  
RST 3  
SHLD LBOP  
TXINT: LHD LBOP  
INCRB 1  
MOV A,1  
RST 3  
SHLD LBOP  
MOV A,M  
CALL CHOUT ; OUTPUT DATA AT LBOP  
LXI H,OUT-COUNT  
M  
JNZ TXINT  
CALL UPSCRN  
RET

08C4 3E9F 08C6 320310 08C9 C3B508  
FULL:  
MOV A,0FFH  
STA TROFLO  
JMP EXIT  
DISPATCH:  
NEXTIN  
RST 4  
RZ  
MOV A,M  
STA OUT-COUNT  
INCRB 3  
MOV A,3  
RST 3  
SHLD LBOP  
TXINT: LHD LBOP  
INCRB 1  
MOV A,1  
RST 3  
SHLD LBOP  
MOV A,M  
CALL CHOUT ; OUTPUT DATA AT LBOP  
LXI H,OUT-COUNT  
M  
JNZ TXINT  
CALL UPSCRN  
RET  
08F0 F5 CLEAR: PUSH PSW

[illegible]



From LIP

VADCG TERMINAL NOTE COMMUNICATIONS PROGRAM - MODULE 1-11

CP/M MACRO ASSEM 2.0 #013

VADCG TERMINAL MOD

CP/M MACRO ASSEM 2.0 #012

```
0891 C9      RET
0892 D630    R00IG: SUI
0893 C9      RET
0894 C9      RET
0895 C9      RET
0896 C9      RET
0897 C9      RET
0898 C9      RET
0899 C9      RET
0900 C9      RET
0901 C9      RET
0902 C9      RET
0903 C9      RET
0904 C9      RET
0905 C9      RET
0906 C9      RET
0907 C9      RET
0908 C9      RET
0909 C9      RET
0910 C9      RET
0911 C9      RET
0912 C9      RET
0913 C9      RET
0914 C9      RET
0915 C9      RET
0916 C9      RET
0917 C9      RET
0918 C9      RET
0919 C9      RET
0920 C9      RET
0921 C9      RET
0922 C9      RET
0923 C9      RET
0924 C9      RET
0925 C9      RET
0926 C9      RET
0927 C9      RET
0928 C9      RET
0929 C9      RET
0930 C9      RET
0931 C9      RET
0932 C9      RET
0933 C9      RET
0934 C9      RET
0935 C9      RET
0936 C9      RET
0937 C9      RET
0938 C9      RET
0939 C9      RET
0940 C9      RET
0941 C9      RET
0942 C9      RET
0943 C9      RET
0944 C9      RET
0945 C9      RET
0946 C9      RET
0947 C9      RET
0948 C9      RET
0949 C9      RET
0950 C9      RET
0951 C9      RET
0952 C9      RET
0953 C9      RET
0954 C9      RET
0955 C9      RET
0956 C9      RET
0957 C9      RET
0958 C9      RET
0959 C9      RET
0960 C9      RET
0961 C9      RET
0962 C9      RET
0963 C9      RET
0964 C9      RET
0965 C9      RET
0966 C9      RET
0967 C9      RET
0968 C9      RET
0969 C9      RET
0970 C9      RET
0971 C9      RET
0972 C9      RET
0973 C9      RET
0974 C9      RET
0975 C9      RET
0976 C9      RET
0977 C9      RET
0978 C9      RET
0979 C9      RET
0980 C9      RET
0981 C9      RET
0982 C9      RET
0983 C9      RET
0984 C9      RET
0985 C9      RET
0986 C9      RET
0987 C9      RET
0988 C9      RET
0989 C9      RET
0990 C9      RET
0991 C9      RET
0992 C9      RET
0993 C9      RET
0994 C9      RET
0995 C9      RET
0996 C9      RET
0997 C9      RET
0998 C9      RET
0999 C9      RET
1000 C9      RET
```

```
0070' 21 0000'
0071' 46
0072' 23
0073' DB 10
0074' 07
0075' DA 0082'
0076' 7E
0077' 03 10
0078' 78
0079' A7
```

issue commands to 8273

VADCG TERMINAL NOTE COMMUNICATIONS PROGRAM  
LIP-SUBROUTINES MODULE  
MACRO-80 3.36 17-Mar-80 PAGE 1-3

```
0080' C8
0081' 23
0082' 05
0083' DB 10
0084' E6 20
0085' C2 0090'
0086' 7E
0087' D3 11
0088' C3 008B'
```

```
0090' DB 10
0091' E6 10
0092' CA 009D'
0093' DB 11
0094' C9
```

```
0095' DB 10
0096' E6 10
0097' CA 009D'
0098' DB 11
0099' C9
```

PAGE 1-3

MESSAGE AREA

MESSAGE AREA

[illegible]

```

006B' C3 0000$
;
RSTEND EQU $
RSTLEN EQU RSTEND-RSTTAB
;
; MEMORY CONFIGURATION EQUATES
;
; LORAM depends on the length of the kluge table
;
LORAM EQU ACTRAM+RSTLEN ; FIRST BYTE OF CONTIGUOUS RAM AREA
HIRAM EQU ACTRAM+OFFFH ; LAST BYTE OF CONTIGUOUS RAM AREA
;
INCLUDE CCA.DEF
; COMMON COMMUNICATIONS AREA PUBLIC DECLARATIONS AND DEFINITIONS
;
;
;
;
INCLUDE STATUS.DEF
; STATUS BIT DEFINITIONS FOR STAT1,2,3 AND CRUF
;
;
PAGE PGSIZ

```

```

; INITIALIZATION CODE
; ENTERED FROM RESTART INTERRUPT
;
;
INIT: DI ; DISABLE INTERRUPTS
;
; MOVE THE RST DISPATCH TABLE TO RAM
;
LXI D,RSTTAB ; GET ADDRESS OF SOURCE FOR MOVE
LXI H,ACTRAM ; GET ADDRESS FOR DESTINATION
MVI R,RSTLEN ; GET COUNT OF ITEMS TO MOVE
RSTMov:
LDAX D ; FETCH A BYTE TO MOVE
MOV M,A ; STORE AT DESTINATION
INX D ; UPDATE SOURCE POINTER
INX H ; AND DESTINATION POINTER
DCR B ; COUNT OFF THE BYTE
JNZ RSTMov
;
LXI D,HIRAM ; HIGHEST ADDRESS TO CLEAR
LXI H,LORAM ; LOWEST ADDRESS TO CLEAR
CLEAR:
MVI M,0
INX H
MOV A,D
CMP H
JNZ CLEAR ; NOT OVER YET
MOV A,E
CMP L
JNZ CLEAR ; NOT OVER YET
; SET UP STACK POINTER
LXI SP,STACK
;
; INITIALIZ LINE BUFFER VARIABLES
LXI H,LBA
SHLD CLBE ; CURRENT LINE BUFFER ENTRY
SHLD OLBE ; OLDEST LINE BUFFER ENTRY
SHLD LRPE ; LINE BUFFER PROCESSING ENTRY
LXI H,LBA+3 ; POINT TO END OF HEADER AREA
SHLD LRIP ; LINE BUFFER INPUT POINTER
;
; INITIALIZE TERMINAL BUFFER VARIABLES
LXI H,TBA ; POINT TO START OF TERMINAL BUFFER AREA
SHLD OTRE ; OLDEST TERMINAL BUFFER ENTRY
SHLD CTBIE ; SET UP CURRENT TERMINAL BUFFER INPUT ENTRY ADDRESS
INX H ; INCREMENT ADDRESS BY ONE
; TO POINT TO END OF HEADER
SHLD TBIP ; TERMINAL BUFFER INPUT POINTER
;
; INITIALIZE CONNECT BUFFER
LXI H,CRUF
LXI D,RTMBUF
MVI B,B ; B<-- LENGTH OF INITIALIZATION DATA

```

*Remainder unchanged...*



```
0050' 5F      MOV     E+4  
0051' 7A      MOV     A+D  
0052' 2F      CMA  
0053' 3C      INR     A  
0054' BR      CMP     E  
0055' C2 008C' JNZ     ERROR  
0056' CD 0080' JNZ     CHRIN  
0057' FE 3A   CFI     ''  
0058' C2 0058' JNZ     ..L02  
0059' C3 0029' JMP     LOADER  
0060'          ;  
0061'          ; UTILITIES  
0062'          ;  
0063' C5      RBYTE: PUSH B  
0064' CD 0072' CALL    RHEX  
0065' 07      RLC  
0066' 07      RLC  
0067' 07      RLC  
0068' 07      RLC  
0069' 07      RLC  
0070' 07      RLC  
0071' 07      RLC  
0072' 47      MOV     B+A  
0073' CD 0072' CALL    RHEX  
0074' B0      DRA     B  
0075' C1      POP     B  
0076' C9      RET  
0077'          ;  
0078' RHEX: CALL    CHRIN  
0079' 9+1     CPI     '9'+1  
0080' DA 007D' JC      R0D1G  
0081' D6 37   SUI     'A'-10  
0082' C9      RET  
0083'          ;  
0084' R0D1G: SUI     '0'  
0085' D6 30   RET  
0086' C9      ;  
0087' CHRIN: IN      LSR  
0088' 01      I  
0089' ANI     1  
0090' JZ      CHRIN  
0091' IN      RBR  
0092' ANI     07FH  
0093' C9      RET  
0094'          ;  
0095' ERROR: CALL    FLASHD  
0096' C3 008C' JMP  
0097'          ;  
0098' FLASH: MVI     A+040H  
0099' 3E 40   :MAKE SOUT LOW TO TURN LED ON  
0100' 30      :TURN IT ON  
0101' SIN  
0102' CALL    DELAY  
0103' 080H    :WAIT A BIT  
0104' ORI     080H  
0105' SIM     :RAISE SOUT LINE TO TURN LED OFF  
0106' :DO IT  
0107' CALL    DELAY  
0108' RET  
0109'          ;  
0110' FLASHB: MVI     A+OUT2  
0111' 03 04   :GET BIT FOR OUT2 LED ON B250  
0112' OUT     MCR  
0113' CALL    DELAY  
0114' XRA     A  
0115' OUT     MCR
```

```
0049' C0 0013' CALL    DELAY  
0050' C9      RET  
0051'          ;  
0052' FLASHB: LXI     H+CMD3  
0053' 21 00E6' :GET COMMAND SEQUENCE FOR LED 'D' ON ON 8273  
0054' CD 0000* CHOUT  
0055' C0 0013' CALL    DELAY  
0056' LXI     H+CMD4  
0057' 21 00E9' :LED 'D' OFF  
0058' CD 0000* CHOUT  
0059' C0 0013' CALL    DELAY  
0060' C9      RET  
0061'          ;  
0062' FLASHB: LXI     H+CMD1  
0063' 21 00E0' :GET COMMAND FOR LED 'E' ON  
0064' CD 0000* CHOUT  
0065' C0 0013' CALL    DELAY  
0066' LXI     H+CMD2  
0067' 21 00E3' :COMMAND LED 'E' OFF  
0068' CD 0000* CHOUT  
0069' C0 0013' CALL    DELAY  
0070' C9      RET  
0071'          ;  
0072' DELAY: MVI     H+50  
0073' 26 32   L+0  
0074' 2E 00   L  
0075' 20      :..L04  
0076' DCR     L  
0077' JNZ     ..L04  
0078' H  
0079' JNZ     ..L03  
0080' C9      RET  
0081'          ;  
0082'          ; COMMAND FOR LINES ON AND OFF  
0083'          ;  
0084' CMD1: 1+0A3H+010H :LED 'D' (PR3) ON  
0085' 01 A3 10  
0086' 01 63 EF :LED 'D' OFF (PR3 LOW)  
0087' 01 A3 08 :LED 'E' ON (PR4 HIGH)  
0088' 01 63 F7 :LED 'E' OFF  
0089'          ;  
0090'          ;  
0091'          ;  
0092'          ;  
0093'          ;  
0094'          ;  
0095'          ;  
0096'          ;  
0097'          ;  
0098'          ;  
0099'          ;  
0100'          ;  
0101'          ;  
0102'          ;  
0103'          ;  
0104'          ;  
0105'          ;  
0106'          ;  
0107'          ;  
0108'          ;  
0109'          ;  
0110'          ;  
0111'          ;  
0112'          ;  
0113'          ;  
0114'          ;  
0115'          ;  
0116'          ;  
0117'          ;  
0118'          ;  
0119'          ;  
0120'          ;  
0121'          ;  
0122'          ;  
0123'          ;  
0124'          ;  
0125'          ;  
0126'          ;  
0127'          ;  
0128'          ;  
0129'          ;  
0130'          ;  
0131'          ;  
0132'          ;  
0133'          ;  
0134'          ;  
0135'          ;  
0136'          ;  
0137'          ;  
0138'          ;  
0139'          ;  
0140'          ;  
0141'          ;  
0142'          ;  
0143'          ;  
0144'          ;  
0145'          ;  
0146'          ;  
0147'          ;  
0148'          ;  
0149'          ;  
0150'          ;  
0151'          ;  
0152'          ;  
0153'          ;  
0154'          ;  
0155'          ;  
0156'          ;  
0157'          ;  
0158'          ;  
0159'          ;  
0160'          ;  
0161'          ;  
0162'          ;  
0163'          ;  
0164'          ;  
0165'          ;  
0166'          ;  
0167'          ;  
0168'          ;  
0169'          ;  
0170'          ;  
0171'          ;  
0172'          ;  
0173'          ;  
0174'          ;  
0175'          ;  
0176'          ;  
0177'          ;  
0178'          ;  
0179'          ;  
0180'          ;  
0181'          ;  
0182'          ;  
0183'          ;  
0184'          ;  
0185'          ;  
0186'          ;  
0187'          ;  
0188'          ;  
0189'          ;  
0190'          ;  
0191'          ;  
0192'          ;  
0193'          ;  
0194'          ;  
0195'          ;  
0196'          ;  
0197'          ;  
0198'          ;  
0199'          ;  
0200'          ;  
0201'          ;  
0202'          ;  
0203'          ;  
0204'          ;  
0205'          ;  
0206'          ;  
0207'          ;  
0208'          ;  
0209'          ;  
0210'          ;  
0211'          ;  
0212'          ;  
0213'          ;  
0214'          ;  
0215'          ;  
0216'          ;  
0217'          ;  
0218'          ;  
0219'          ;  
0220'          ;  
0221'          ;  
0222'          ;  
0223'          ;  
0224'          ;  
0225'          ;  
0226'          ;  
0227'          ;  
0228'          ;  
0229'          ;  
0230'          ;  
0231'          ;  
0232'          ;  
0233'          ;  
0234'          ;  
0235'          ;  
0236'          ;  
0237'          ;  
0238'          ;  
0239'          ;  
0240'          ;  
0241'          ;  
0242'          ;  
0243'          ;  
0244'          ;  
0245'          ;  
0246'          ;  
0247'          ;  
0248'          ;  
0249'          ;  
0250'          ;  
0251'          ;  
0252'          ;  
0253'          ;  
0254'          ;  
0255'          ;  
0256'          ;  
0257'          ;  
0258'          ;  
0259'          ;  
0260'          ;  
0261'          ;  
0262'          ;  
0263'          ;  
0264'          ;  
0265'          ;  
0266'          ;  
0267'          ;  
0268'          ;  
0269'          ;  
0270'          ;  
0271'          ;  
0272'          ;  
0273'          ;  
0274'          ;  
0275'          ;  
0276'          ;  
0277'          ;  
0278'          ;  
0279'          ;  
0280'          ;  
0281'          ;  
0282'          ;  
0283'          ;  
0284'          ;  
0285'          ;  
0286'          ;  
0287'          ;  
0288'          ;  
0289'          ;  
0290'          ;  
0291'          ;  
0292'          ;  
0293'          ;  
0294'          ;  
0295'          ;  
0296'          ;  
0297'          ;  
0298'          ;  
0299'          ;  
0300'          ;  
0301'          ;  
0302'          ;  
0303'          ;  
0304'          ;  
0305'          ;  
0306'          ;  
0307'          ;  
0308'          ;  
0309'          ;  
0310'          ;  
0311'          ;  
0312'          ;  
0313'          ;  
0314'          ;  
0315'          ;  
0316'          ;  
0317'          ;  
0318'          ;  
0319'          ;  
0320'          ;  
0321'          ;  
0322'          ;  
0323'          ;  
0324'          ;  
0325'          ;  
0326'          ;  
0327'          ;  
0328'          ;  
0329'          ;  
0330'          ;  
0331'          ;  
0332'          ;  
0333'          ;  
0334'          ;  
0335'          ;  
0336'          ;  
0337'          ;  
0338'          ;  
0339'          ;  
0340'          ;  
0341'          ;  
0342'          ;  
0343'          ;  
0344'          ;  
0345'          ;  
0346'          ;  
0347'          ;  
0348'          ;  
0349'          ;  
0350'          ;  
0351'          ;  
0352'          ;  
0353'          ;  
0354'          ;  
0355'          ;  
0356'          ;  
0357'          ;  
0358'          ;  
0359'          ;  
0360'          ;  
0361'          ;  
0362'          ;  
0363'          ;  
0364'          ;  
0365'          ;  
0366'          ;  
0367'          ;  
0368'          ;  
0369'          ;  
0370'          ;  
0371'          ;  
0372'          ;  
0373'          ;  
0374'          ;  
0375'          ;  
0376'          ;  
0377'          ;  
0378'          ;  
0379'          ;  
0380'          ;  
0381'          ;  
0382'          ;  
0383'          ;  
0384'          ;  
0385'          ;  
0386'          ;  
0387'          ;  
0388'          ;  
0389'          ;  
0390'          ;  
0391'          ;  
0392'          ;  
0393'          ;  
0394'          ;  
0395'          ;  
0396'          ;  
0397'          ;  
0398'          ;  
0399'          ;  
0400'          ;  
0401'          ;  
0402'          ;  
0403'          ;  
0404'          ;  
0405'          ;  
0406'          ;  
0407'          ;  
0408'          ;  
0409'          ;  
0410'          ;  
0411'          ;  
0412'          ;  
0413'          ;  
0414'          ;  
0415'          ;  
0416'          ;  
0417'          ;  
0418'          ;  
0419'          ;  
0420'          ;  
0421'          ;  
0422'          ;  
0423'          ;  
0424'          ;  
0425'          ;  
0426'          ;  
0427'          ;  
0428'          ;  
0429'          ;  
0430'          ;  
0431'          ;  
0432'          ;  
0433'          ;  
0434'          ;  
0435'          ;  
0436'          ;  
0437'          ;  
0438'          ;  
0439'          ;  
0440'          ;  
0441'          ;  
0442'          ;  
0443'          ;  
0444'          ;  
0445'          ;  
0446'          ;  
0447'          ;  
0448'          ;  
0449'          ;  
0450'          ;  
0451'          ;  
0452'          ;  
0453'          ;  
0454'          ;  
0455'          ;  
0456'          ;  
0457'          ;  
0458'          ;  
0459'          ;  
0460'          ;  
0461'          ;  
0462'          ;  
0463'          ;  
0464'          ;  
0465'          ;  
0466'          ;  
0467'          ;  
0468'          ;  
0469'          ;  
0470'          ;  
0471'          ;  
0472'          ;  
0473'          ;  
0474'          ;  
0475'          ;  
0476'          ;  
0477'          ;  
0478'          ;  
0479'          ;  
0480'          ;  
0481'          ;  
0482'          ;  
0483'          ;  
0484'          ;  
0485'          ;  
0486'          ;  
0487'          ;  
0488'          ;  
0489'          ;  
0490'          ;  
0491'          ;  
0492'          ;  
0493'          ;  
0494'          ;  
0495'          ;  
0496'          ;  
0497'          ;  
0498'          ;  
0499'          ;  
0500'          ;  
0501'          ;  
0502'          ;  
0503'          ;  
0504'          ;  
0505'          ;  
0506'          ;  
0507'          ;  
0508'          ;  
0509'          ;  
0510'          ;  
0511'          ;  
0512'          ;  
0513'          ;  
0514'          ;  
0515'          ;  
0516'          ;  
0517'          ;  
0518'          ;  
0519'          ;  
0520'          ;  
0521'          ;  
0522'          ;  
0523'          ;  
0524'          ;  
0525'          ;  
0526'          ;  
0527'          ;  
0528'          ;  
0529'          ;  
0530'          ;  
0531'          ;  
0532'          ;  
0533'          ;  
0534'          ;  
0535'          ;  
0536'          ;  
0537'          ;  
0538'          ;  
0539'          ;  
0540'          ;  
0541'          ;  
0542'          ;  
0543'          ;  
0544'          ;  
0545'          ;  
0546'          ;  
0547'          ;  
0548'          ;  
0549'          ;  
0550'          ;  
0551'          ;  
0552'          ;  
0553'          ;  
0554'          ;  
0555'          ;  
0556'          ;  
0557'          ;  
0558'          ;  
0559'          ;  
0560'          ;  
0561'          ;  
0562'          ;  
0563'          ;  
0564'          ;  
0565'          ;  
0566'          ;  
0567'          ;  
0568'          ;  
0569'          ;  
0570'          ;  
0571'          ;  
0572'          ;  
0573'          ;  
0574'          ;  
0575'          ;  
0576'          ;  
0577'          ;  
0578'          ;  
0579'          ;  
0580'          ;  
0581'          ;  
0582'          ;  
0583'          ;  
0584'          ;  
0585'          ;  
0586'          ;  
0587'          ;  
0588'          ;  
0589'          ;  
0590'          ;  
0591'          ;  
0592'          ;  
0593'          ;  
0594'          ;  
0595'          ;  
0596'          ;  
0597'          ;  
0598'          ;  
0599'          ;  
0600'          ;  
0601'          ;  
0602'          ;  
0603'          ;  
0604'          ;  
0605'          ;  
0606'          ;  
0607'          ;  
0608'          ;  
0609'          ;  
0610'          ;  
0611'          ;  
0612'          ;  
0613'          ;  
0614'          ;  
0615'          ;  
0616'          ;  
0617'          ;  
0618'          ;  
0619'          ;  
0620'          ;  
0621'          ;  
0622'          ;  
0623'          ;  
0624'          ;  
0625'          ;  
0626'          ;  
0627'          ;  
0628'          ;  
0629'          ;  
0630'          ;  
0631'          ;  
0632'          ;  
0633'          ;  
0634'          ;  
0635'          ;  
0636'          ;  
0637'          ;  
0638'          ;  
0639'          ;  
0640'          ;  
0641'          ;  
0642'          ;  
0643'          ;  
0644'          ;  
0645'          ;  
0646'          ;  
0647'          ;  
0648'          ;  
0649'          ;  
0650'          ;  
0651'          ;  
0652'          ;  
0653'          ;  
0654'          ;  
0655'          ;  
0656'          ;  
0657'          ;  
0658'          ;  
0659'          ;  
0660'          ;  
0661'          ;  
0662'          ;  
0663'          ;  
0664'          ;  
0665'          ;  
0666'          ;  
0667'          ;  
0668'          ;  
0669'          ;  
0670'          ;  
0671'          ;  
0672'          ;  
0673'          ;  
0674'          ;  
0675'          ;  
0676'          ;  
0677'          ;  
0678'          ;  
0679'          ;  
0680'          ;  
0681'          ;  
0682'          ;  
0683'          ;  
0684'          ;  
0685'          ;  
0686'          ;  
0687'          ;  
0688'          ;  
0689'          ;  
0690'          ;  
0691'          ;  
0692'          ;  
0693'          ;  
0694'          ;  
0695'          ;  
0696'          ;  
0697'          ;  
0698'          ;  
0699'          ;  
0700'          ;  
0701'          ;  
0702'          ;  
0703'          ;  
0704'          ;  
0705'          ;  
0706'          ;  
0707'          ;  
0708'          ;  
0709'          ;  
0710'          ;  
0711'          ;  
0712'          ;  
0713'          ;  
0714'          ;  
0715'          ;  
0716'          ;  
0717'          ;  
0718'          ;  
0719'          ;  
0720'          ;  
0721'          ;  
0722'          ;  
0723'          ;  
0724'          ;  
0725'          ;  
0726'          ;  
0727'          ;  
0728'          ;  
0729'          ;  
0730'          ;  
0731'          ;  
0732'          ;  
0733'          ;  
0734'          ;  
0735'          ;  
0736'          ;  
0737'          ;  
0738'          ;  
0739'          ;  
0740'          ;  
0741'          ;  
0742'          ;  
0743'          ;  
0744'          ;  
0745'          ;  
0746'          ;  
0747'          ;  
0748'          ;  
0749'          ;  
0750'          ;  
0751'          ;  
0752'          ;  
0753'          ;  
0754'          ;  
0755'          ;  
0756'          ;  
0757'          ;  
0758'          ;  
0759'          ;  
0760'          ;  
0761'          ;  
0762'          ;  
0763'          ;  
0764'          ;  
0765'          ;  
0766'          ;  
0767'          ;  
0768'          ;  
0769'          ;  
0770'          ;  
0771'          ;  
0772'          ;  
0773'          ;  
0774'          ;  
0775'          ;  
0776'          ;  
0777'          ;  
0778'          ;  
0779'          ;  
0780'          ;  
0781'          ;  
0782'          ;  
0783'          ;  
0784'          ;  
0785'          ;  
0786'          ;  
0787'          ;  
0788'          ;  
0789'          ;  
0790'          ;  
0791'          ;  
0792'          ;  
0793'          ;  
0794'          ;  
0795'          ;  
0796'          ;  
0797'          ;  
0798'          ;  
0799'          ;  
0800'          ;  
0801'          ;  
0802'          ;  
0803'          ;  
0804'          ;  
0805'          ;  
0806'          ;  
0807'          ;  
0808'          ;  
0809'          ;  
0810'          ;  
0811'          ;  
0812'          ;  
0813'          ;  
0814'          ;  
0815'          ;  
0816'          ;  
0817'          ;  
0818'          ;  
0819'          ;  
0820'          ;  
0821'          ;  
0822'          ;  
0823'          ;  
0824'          ;  
0825'          ;  
0826'          ;  
0827'          ;  
0828'          ;  
0829'          ;  
0830'          ;  
0831'          ;  
0832'          ;  
0833'          ;  
0834'          ;  
0835'          ;  
0836'          ;  
0837'          ;  
0838'          ;  
0839'          ;  
0840'          ;  
0841'          ;  
0842'          ;  
0843'          ;  
0844'          ;  
0845'          ;  
0846'          ;  
0847'          ;  
0848'          ;  
0849'          ;  
0850'          ;  
0851'          ;  
0852'          ;  
0853'          ;  
0854'          ;  
0855'          ;  
0856'          ;  
0857'          ;  
0858'          ;  
0859'          ;  
0860'          ;  
0861'          ;  
0862'          ;  
0863'          ;  
0864'          ;  
0865'          ;  
0866'          ;  
0867'          ;  
0868'          ;  
0869'          ;  
0870'          ;  
0871'          ;  
0872'          ;  
0873'          ;  
0874'          ;  
0875'          ;  
0876'          ;  
0877'          ;  
0878'          ;  
0879'          ;  
0880'          ;  
0881'          ;  
0882'          ;  
0883'          ;  
0884'          ;  
0885'          ;  
0886'          ;  
0887'          ;  
0888'          ;  
0889'          ;  
0890'          ;  
0891'          ;  
0892'          ;  
0893'          ;  
0894'          ;  
0895'          ;  
0896'          ;  
0897'          ;  
0898'          ;  
0899'          ;  
0900'          ;  
0901'          ;  
0902'          ;  
0903'          ;  
0904'          ;  
0905'          ;  
0906'          ;  
0907'          ;  
0908'          ;  
0909'          ;  
0910'          ;  
0911'          ;  
0912'          ;  
0913'          ;  
0914'          ;  
0915'          ;  
0916'          ;  
0917'          ;  
0918'          ;  
0919'          ;  
0920'          ;  
0921'          ;  
0922'          ;  
0923'          ;  
0924'          ;  
0925'          ;  
0926'          ;  
0927'          ;  
0928'          ;  
0929'          ;  
0930'          ;  
0931'          ;  
0932'          ;  
0933'          ;  
0934'          ;  
0935'          ;  
0936'          ;  
0937'          ;  
0938'          ;  
0939'          ;  
0940'          ;  
0941'          ;  
0942'          ;  
0943'          ;  
0944'          ;  
0945'          ;  
0946'          ;  
0947'          ;  
0948'          ;  
0949'          ;  
0950'          ;  
0951'          ;  
0952'          ;  
0953'          ;  
0954'          ;  
0955'          ;  
0956'          ;  
0957'          ;  
0958'          ;  
0959'          ;  
0960'          ;  
0961'          ;  
0962'          ;  
0963'          ;  
0964'          ;  
0965'          ;  
0966'          ;  
0967'          ;  
0968'          ;  
0969'          ;  
0970'          ;  
0971'          ;  
0972'          ;  
0973'          ;  
0974'          ;  
0975'          ;  
0976'          ;  
0977'          ;  
0978'          ;  
0979'          ;  
0980'          ;  
0981'          ;  
0982'          ;  
0983'          ;  
0984'          ;  
0985'          ;  
0986'          ;  
0987'          ;  
0988'          ;  
0989'          ;  
0990'          ;  
0991'          ;  
0992'          ;  
0993'          ;  
0994'          ;  
0995'          ;  
0996'          ;  
0997'          ;  
0998'          ;  
0999'          ;  
1000'          ;  
1001'          ;  
1002'          ;  
1003'          ;  
1004'          ;  
1005'          ;  
1006'          ;  
1007'          ;  
1008'          ;  
1009'          ;  
1010'          ;  
1011'          ;  
1012'          ;  
1013'          ;  
1014'          ;  
1015'          ;  
1016'          ;  
1017'          ;  
1018'          ;  
1019'          ;  
1020'          ;  
1021'          ;  
1022'          ;  
1023'          ;  
1024'          ;  
1025'          ;  
1026'          ;  
1027'          ;  
1028'          ;  
1029'          ;  
1030'          ;  
1031'          ;  
1032'          ;  
1033'          ;  
1034'          ;  
1035'          ;  
1036'          ;  
1037'          ;  
1038'          ;  
1039'          ;  
1040'          ;  
1041'          ;  
1042'          ;  
1043'          ;  
1044'          ;  
1045'          ;  
1046'          ;  
1047'          ;  
1048'          ;  
1049'          ;  
1050'          ;  
1051'          ;  
1052'          ;  
1053'          ;  
1054'          ;  
1055'          ;  
1056'          ;  
1057'          ;  
1058'          ;  
1059'          ;  
1060'          ;  
1061'          ;  
1062'          ;  
1063'          ;  
1064'          ;  
1065'          ;  
1066'          ;  
1067'          ;  
1068'          ;  
1069'          ;  
1070'          ;  
1071'          ;  
1072'          ;  
1073'          ;  
1074'          ;  
1075'          ;  
1076'          ;  
1077'          ;  
1078'          ;  
1079'          ;  
1080'          ;  
1081'          ;  
1082'          ;  
1083'          ;  
1084'          ;  
1085'          ;  
1086'          ;  
1087'          ;  
1088'          ;  
1089'          ;  
1090'          ;  
1091'          ;  
1092'          ;  
1093'          ;  
1094'          ;  
1095'          ;  
1096'          ;  
1097'          ;  
1098'          ;  
1099'          ;  
1100'          ;  
1101'          ;  
1102'          ;  
1103'          ;  
1104'          ;  
1105'          ;  
1106'          ;  
1107'          ;  
1108'          ;  
1109'          ;  
1110'          ;  
1111'          ;  
1112'          ;  
1113'          ;  
1114'          ;  
1115'          ;  
1116'          ;  
1117'          ;  
1118'          ;  
1119'          ;  
1120'          ;  
1121'          ;  
1122'          ;  
1123'          ;  
1124'          ;  
1125'          ;  
1126'          ;  
1127'          ;  
1128'          ;  
1129'         
```

# \* - PEOPLE AT JAN 25th Meeting

>TYPE MAILLIST.  
 \*\* DM0:LI,76JMAILLIST,i21 -- Last written 26-JAN-81 14:49:16 \*\*

\*

\$\$\$  
 Robert Sleath, VES3EFT,  
 1275 Eisin St., #1402,  
 Burlington, Ontario.

+ H 632-6279 0 637-4515  
 64 character display, terminal only. Runs off  
 Yeasu synthesized voice. Mini monitor in terminal  
 node. Uses parallel interface to keyboard and display.  
 Interested in packet voice and access to other computer  
 systems.

\$\$\$  
 Brian Kennedy, VS9ASP  
 90 Sarah Lane, Unit #3,  
 Oakville, Ontario,  
 L6L 5L3.

+ H 825-0925 0 865-4427  
 TRS-80 system.

\$\$\$  
 AMRAD Corp.,  
 1524 Spring Vale Avenue,  
 McLean, Virginia, 22101.

+ Swap bulletins

\$\$\$  
 Dr. Thomas A. Dwyer,  
 Soloworks Laboratory,  
 Dept. Computer Science,  
 University of Pittsburgh,  
 Pittsburgh, PA, 15260.

+ distributed applications a la N-TREX.  
 send information re multi-user implementations.

\$\$\$  
 John Vander Biers, VES3NVV,  
 RR #2, Group G, Box 14,  
 Mount Hope, Ontario,  
 L0R 1W0.

\*

+ H 692-3802 0 528-8447

Down loadable terminal node on homebrew Z-80 CP/M system.  
 Super monitor package for monitoring and running  
 the TNC. Has remote console on his system.  
 Interested in digital picture transmission and graphics.

\$\$\$  
 Stewart Beal, SWL.  
 2391 Arnold Cres.,  
 Burlington, Ontario,  
 L7P 4J2.

\*

+ H 335-3461 0 637-4373

TNC on CP/M system. System also has 8273 on S-100  
 card for station mode controller. Interested in  
 interactive color graphics, message switching, packet video.

\*

Write code primarily in C.  
 \$\$\$  
 Frank Roberts, VES3FAO  
 27 Willis Dr.,  
 Brampton, Ontario,  
 L6W 1A8.

+ H 457-9583 0 270-3030 x276  
 Professionally involved with digital communications since '64.  
 Has 202 modem, dumb terminal and VADICG board but no power  
 supply. Interested in digital TV.

\$\$\$  
 Brian Brownlee,  
 898 Francis Road,  
 Burlington, Ontario,  
 L7T 3Y2.

\*

+ H 634-1470 0 637-4221  
 TRS-80. Currently working on S-100 system. Not  
 an amateur but interested in the software.  
 Experience with CBRS and is active in Burlington  
 microcomputer club

\$\$\$  
 Max Pizzolato, VES3DNH  
 65 Elgar Ave.,  
 Hamilton, Ontario,  
 L9C 4E4.

\*

+ H 385-2530  
 TNC board nearing completion. TRS-80 system.

\$\$\$  
 Fulko Hew,  
 6650 Twiss Road, RR #3,  
 Campbellville, Ontario,  
 L0P 1R0.

\*

+ H 335-3033 0 528-8811 x4242  
 Altair system, 1 floppy, interested in graphics and  
 high speed communication.

\$\$\$  
 Glenn Simpson, VES3DSP  
 61 Briarwood Cres.,  
 Hamilton, Ontario,  
 L9C 4C3.

\*

+ H 385-8478 0 528-0811 x3122  
 TNC nearing completion. TRS-80 and 1802 system.  
 Interested in satellite links and (later) packet  
 voice.

\$\$\$  
 Dan Robertson, VES3FOV,  
 32 George Henry Blvd.,  
 Willowdale, Ontario,  
 M2V 1E2.

\*

+ H 494-7288 0 499-5050

MCM-800 MPL machine. Interested in CBRS  
 \$\$\$  
 W.J. Montgomery, VES3EC

\*

8 McCordick Drive,  
 St. Catharines, Ontario,  
 L2N 6S3.  
 +  
 H 934-6303 0 637-4515  
 TNC on CP/M system. Interested in Color interactive  
 graphics, file transfer. Uses C and Pascal  
 \$\$\$  
 James Knott, VE3CVM  
 55 Park St., #1402,  
 Mississauga, Ontario,  
 L5G 1L9.  
 +  
 H 279-5399 0 860-5183  
 Imsai 8080 cassette system. Works for CN/CP  
 servicing ITT equipment.  
 \$\$\$  
 Paul Deversaux,  
 1337 Woodvale Place,  
 Burlington, Ontario.  
 +  
 Programmer. interested in network.  
 \$\$\$  
 Michael Connolly, VE3MDC  
 34 Schubert Drive,  
 Scarborough, Ontario,  
 M1E 1Y9.  
 +  
 H 281-0513 0 966-5575  
 with DOC regional office, Toronto. responsible for  
 training radio inspectors. believes weshould provide  
 a standardized protocol among all experimenters  
 rather than isolated cells.  
 \$\$\$  
 Russel S. Milland, VE3FUX  
 12 Princess Margaret Blvd.,  
 Islington, Ontario,  
 M9A 1Z4.  
 +  
 H 231-0252 0 968-4838  
 Z-80 S-100 system running CP/M and PL-1.  
 designed digital systems as engineer, now interested in  
 RTTY, HF experiments, CBRS.  
 \$\$\$  
 Dr. George Piasecki, VE3GUH  
 473 Copeland Court,  
 Oakville, Ontario,  
 L6J 4R8.  
 +  
 H 844-9889 0 844-2444  
 PET machine with dual floppy. interested in CBRS.  
 Member of rather large PET computer club.  
 \$\$\$  
 Tom Gleason, VE3MFC (W9ITI)  
 +  
 member of PET club.  
 \$\$\$  
 Keith Witney, VE3DYW  
 740 York Mills Rd., #1508,  
 Don Mills, Ontario.  
 +  
 cannot locate this person.  
 \$\$\$  
 Clayt Anquish, VE3LU  
 900 Colborne St.,  
 Brantford, Ontario.  
 +  
 H (519) 753-7674  
 \$\$\$  
 Glen Leinweber, VE3DNL  
 110 Marlowe Dr.,  
 Hamilton, Ontario,  
 L9C 2H9.  
 +  
 H 389-5658 0 525-9140 x4251  
 IMSAI 8080 system currently used for processing weather  
 satellite pictures. interested in graphics and high-speed  
 communication.  
 \$\$\$  
 Ray Ewan, VE3HMY  
 1058 Joan Drive,  
 Burlington, Ontario,  
 L7T 3H2.  
 +  
 H 634-1712  
 S-100 Z-80 system with 1 floppy and 9T tape.  
 CP/M 1.4  
 \$\$\$  
 Brian Fox, VE3FRF  
 45 Rosedale,  
 Grimsby, Ontario.  
 +  
 H 945-8179 0 561-9311  
 \$\$\$  
 Jeff Knight, VE3VA  
 141 Castlerock Dr.,  
 House #42,  
 Richmond Hill, Ontario,  
 L4C 5N2.  
 +  
 H 884-3299 0 860-2876  
 AIM-65 system.  
 \$\$\$  
 Al Lightstone, VE3LF  
 89 German Mills Rd.,  
 Thornhill, Ontario,  
 L3T 4H9.  
 +  
 H 889-9657 0 223-8191  
 On board of directors RSO. AIM-65 system  
 interested in CBRS and satellite (Phase 3B)  
 >

# AN-01

## THE XR-2207 FSK MODULATOR

- Typically 20 ppm/°C temperature stability
- Phase-continuous FSK output

## INTRODUCTION

Frequency shift keying (FSK) is the most commonly used method for transmitting digital data over telecommunications links. In order to use FSK, a modulator-demodulator (modem) is needed to translate digital 1's and 0's into their respective frequencies and back again.

This Applications Note describes the design of a modem using state-of-the-art Exar devices specifically intended for modem application..

The devices featured in this Application Note are the XR-2206 and XR-2207 FSK modulators, and the XR-2211 FSK demodulator with carrier-detect capability. Because of the superior frequency stability (typically 20 ppm/°C) of these devices, a properly designed circuit will retain its carrier-detect capability. Because of the temperature- and voltage-dependent drift problems associated with many other designs, modern using them will be virtually free of the temperature- and voltage-dependent drift problems associated with many other designs. In addition, the demodulator performance is independent of incoming signal strength variation over a 60 dB dynamic range. Because bias voltages are generated internally, the external parts count is much lower than in most other designs. The modern designs shown in this Applications Note can be used with mark and space frequencies anywhere from several Hertz to 100 kilohertz.

## THE XR-2206 FSK MODULATOR

## FEATURES

- Typically 20 ppm/°C temperature stability
- Choice of 0.5% THD sinewave, triangle, or squarewave output
- Phase-continuous FSK output
- Inputs are TTL and C/MOS compatible
- Low power supply sensitivity (0.01%/V)
- Split or single supply operation
- Low external parts count

## OPERATION

The XR-2206 is ideal for FSK applications requiring the spectral purity of a sinusoidal output waveform. It offers TTL and C/MOS compatibility, excellent frequency stability, and ease of application. The XR-2206 can typically provide a 3 volt p-p sinewave output. Total harmonic distortion can be trimmed to  $\pm 0.5\%$ , if left untrimmed, it is approximately 2.5%.

The circuit connection for the XR-2206 FSK Generator is shown in Figure 1. The data input is applied to pin 9. A high level signal selects the frequency (1/R<sub>6</sub>C<sub>3</sub>) Hz; a low level signal selects the frequency (1/R<sub>7</sub>C<sub>3</sub>) Hz. (resistors in ohms and capacitors in farads). For optimum stability, R<sub>6</sub> and R<sub>7</sub> should be within the range of 10 k $\Omega$  to 100 k $\Omega$ . The voltage applied to pin 9 should be selected to fall between ground and V<sub>+</sub>.

**Note:** Over and under voltage may damage the device

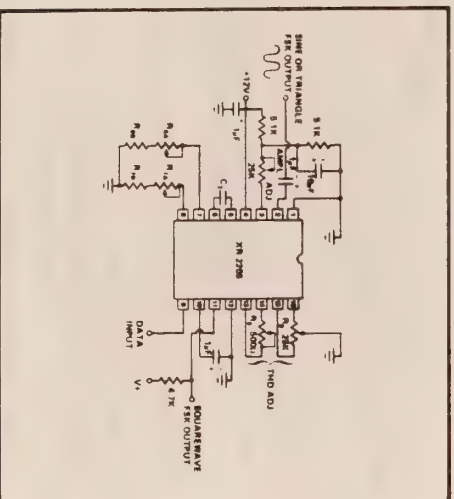


Figure 1. The XR-2206 Sinusoidal FSK Generator

## FEATURES

- Typically 20 ppm/°C temperature stability
- Phase-continuous FSK output
- Provides both triangle and squarewave outputs
- Operates single-channel or two-channel multiplex
- Inputs are TTL and C/MOS compatible
- Split or single power supply operation
- Low power supply sensitivity (0.15%/V)
- Low external parts count

## OPERATION

The XR-2207 is a stable FSK generator which is designed for those applications where only a triangle or squarewave output is required. It is capable of either single-channel or two-channel multiplex operation, and can be used easily with either split or single power supplies.

Figure 2 shows the XR-2207 using a single-supply and Figure 3 shows split-supply operation. When used as an ESK modulator with pins 8 and 9 provide the digital inputs. When the 2207 is used with a split-supply, the threshold at these pins is approximately +2 volts, which is a level that is compatible with both TTL and C/MOS logic forms. When used with a single supply, the threshold is near mid-supply and is C/MOS compatible. Table 1 shows how to select the timing resistors  $R_1$  thru  $R_4$  to determine the output frequency based upon the logic levels applied to pins 8 and 9. For optimum stability, the values of  $R_1$  and  $R_3$  should be selected to fall between 10 k $\Omega$  and 100 k $\Omega$ .

With pin 9 grounded, pin 9 serves as the data input. A high-level signal applied to pin 8 will disable the oscillator. When used in this manner, pin 8 of the XR-2207 serves as the channel select input. For two-channel multiplex operation, pins 4 and 5 should be connected as shown by the dotted lines. (For single-channel operation, pins 4 and 5 should be left open-circuited.)

The XR-2207 provides two outputs; a squarewave at pin 13 and a trianglewave at pin 14. When used with a split-supply, the trianglewave peak-to-peak amplitude is equal to  $V_{-}$  and the dc level is near ground. Direct coupling is usually used. With a single-supply, the peak-to-peak amplitude is approximately equal to  $\frac{1}{2}V_{+}$ , the DC level is at approximately mid-supply and AC coupling is usually necessary. In either case, the output impedance is typically 100 $\Omega$  and is internally protected against short circuits.

The square-wave output has an NPN open-collector configuration. When connected as shown in Figure 2 or 3 this output voltage will swing between V+ and the voltage at pin 12.

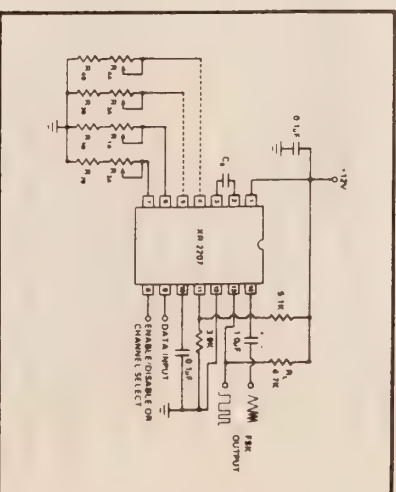


Figure 2 The XR-2207 FSK Modulator Single-Supply Operation

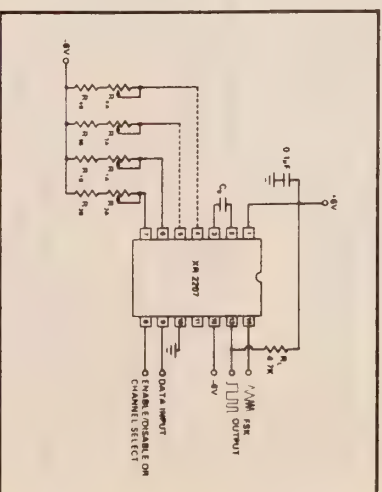


Figure 3. The XR-2207 FSK Modulator Split-Supply Operation

Logic Level		Active Timing Resistor	Output Frequency
Pin 8	Pin 9		
L	L	Pin 6	$\frac{1}{C_0 R_1}$
L	H	Pins 6 and 7	$\frac{1}{C_0 R_1} + \frac{1}{C_0 R_2}$
H	L	Pin 5	$\frac{1}{C_0 R_3}$
H	H	Pins 4 and 5	$\frac{1}{C_0 R_3} + \frac{1}{C_0 R_4}$

Units Resistors — Ohms; Capacitors — Farads; Frequency — Hz

# THE XR-2211 FSK DEMODULATOR WITH CARRIER DETECT

## FEATURES

- Typically 20 ppm/°C temperature stability
- Simultaneous FSK and carrier-detect output
- Outputs are TTL and CMOS compatible
- Wide dynamic range (2 mV to 3 Vrms)
- Split or single supply operation
- Low power supply sensitivity (0.05%/V)
- Low external parts count

## OPERATION

The XR-2211 is a FSK demodulator which operates on the phase-locked-loop principle. Its performance is virtually independent of input signal strength variations over the range of 2 mV to 3 Vrms.

Figure 4 shows the circuit connection for the XR-2211. The center frequency is determined by  $f_0 = (1/C_1 R_4)$  Hz, where capacitance is in farads and resistance is in ohms.  $F_0$  should be calculated to fall midway between the mark and space frequencies.

The tracking range ( $\pm\Delta f$ ) is the range of frequencies over which the phase-locked loop can retain lock with a swept input signal. This range is determined by the formula:  $\Delta f = (R_4 f_0/R_5) \text{ Hz}$ .  $\Delta f$  should be made equal to, or slightly less than, the difference between the mark and space frequencies. For optimum stability, choose an  $R_4$  between 10 k $\Omega$  and 100 k $\Omega$ .

The capture range ( $\pm\Delta f_c$ ) is the range of frequencies over which the phase-locked loop can acquire lock. It is always less than the tracking range. The capture range is limited by  $C_2$ , which, in conjunction with  $R_5$ , forms the loop filter time constant. In most modem applications,  $\Delta f_c = (80\% - 90\%) \Delta f$ .

The loop damping factor ( $\zeta$ ) determines the amount of overshoot, undershoot, or ringing present in the phase-locked loop's response to a step change in frequency. It is determined by  $\zeta = \sqrt{K_d C_1 / C_2}$ . For most modem applications, choose  $\zeta \approx 0.7$ .

## DESIGNING THE MODEM

- Table 2 shows recommended component values for the three most commonly used FSK bands. In many instances, system constraints dictate the use of some non-standard FSK band. The XR-2206/XR-2207, XR-2211 combination is suitable for any range of frequencies from several Hertz to 100 kiloHertz. There are several guidelines to use when calculating non-standard frequencies:

There are several guidelines to use when calculating non-standard frequencies:

The FSK output filter time constant ( $\tau_F$ ) removes chatter from the FSK output. The formula is:  $\tau_F = R_F C_F$ . Normally calculate  $\tau_F$  to be approximately equal to  $[0.3/(\text{baud rate})]$  seconds.

The lock-detect filter capacitor ( $C_D$ ) removes chatter from the lock-detect output. With  $R_D = 510\text{ k}\Omega$ , the minimum value of  $C_D$  can be determined by:  $C_D (\mu\text{F}) \approx 16/\text{capture range in Hz}$ .

**Note:** Excessive values of  $C_D$  will unnecessarily slow the lock-detect response time.

The XR-2211 has three NPN open collector outputs, each of which is capable of sinking up to 5 mA. Pin 7 is the FSK data output, Pin 5 is the Qlock-detect output, which goes low when a carrier is detected, and Pin 6 is the  $\bar{Q}$  lock detect output, which goes high when lock is detected. If pins 6 and 7 are wired together, the output signal from these terminals will provide data when FSK is applied and will be "low" when no carrier is present.

If the lock-detect feature is not required, pins 3, 5 and 6 may be left open-circuited.

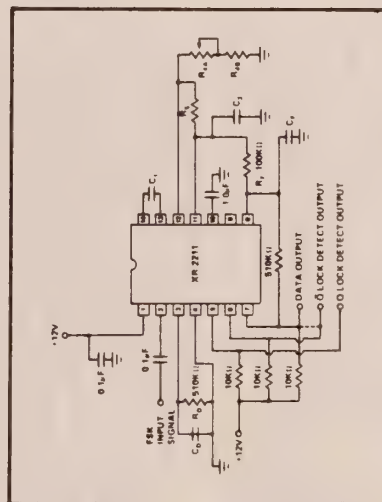


Figure 4. The XR-2211 FSK Demodulator with Carrier Detect

- For maximum baud rate, choose the highest upper frequency that is consistent with the system bandwidth.
- The lower frequency must be at least 55% of the upper frequency. (Less than a 2:1 ratio)
- For minimum demodulated output pulsewidth jitter, select an FSK band whose mark and space frequencies are

For minimum demodulated output pulsewidth jitter, select an FSK band whose mark and space frequencies are

For narrower spacing, the minimum ratio should be about 67%.

- The values shown in Table 2 may be scaled proportionately for mark and space frequencies, maximum baud rate, and (inversely) capacitor value. It is best to retain (approximately) the resistor values shown.

For any given pair of mark and space frequencies, there is a limit to the baud rate that can be achieved. When maximum spacing between the mark and space frequencies is used (where the ratio is close to 2:1) the relationship

should be observed.

**TABLE 2**  
**Recommended Component Values for Typical FSK Bands**

FSK Band			XR-2207				XR-2206				XR-2211								
Band Rate	f <sub>L</sub>	f <sub>H</sub>	R <sub>1A</sub> R <sub>3A</sub>	R <sub>1B</sub> R <sub>3B</sub>	R <sub>2A</sub> R <sub>4A</sub>	R <sub>2B</sub> R <sub>4B</sub>	C <sub>0</sub>	R <sub>6A</sub>	R <sub>6B</sub>	R <sub>7A</sub>	R <sub>7B</sub>	C <sub>3</sub>	R <sub>4A</sub>	R <sub>4B</sub>	R <sub>5</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>F</sub>	C <sub>D</sub>
300	1070	1270	10	20	100	100	.039	10	18	10	20	.039	10	18	100	.039	.01	.0005	.05
300	2025	2225	10	18	150	160	.022	10	16	10	18	.022	10	18	200	.022	.0047	.0005	.05
1200	1200	2200	20	30	20	36	.022	10	16	20	30	.022	10	18	30	.022	.01	.0022	.01

Units: Frequency: Hz: Resistors:  $k\Omega$ : Capacitors:  $\mu F$ 

## DESIGN EXAMPLES

- A. Design a modem to handle a 10 kilobaud data rate, using the minimum necessary bandwidth.
- Frequency Calculation
 

Because we want to use the minimum possible bandwidth (lowest possible upper frequency) we will use a 55:100 frequency ratio. The frequency difference, or 45% of the upper frequency, will be 83% of 10,000. We therefore choose an upper frequency:

$$\frac{83 \times 10,000}{45} = 18,444 \text{ kHz} \approx 18.5 \text{ kHz.}$$

and the lower frequency:

$$0.55 \times 18.5 \text{ kHz} = 10.175 \text{ kHz.}$$
  - Component Selection
    - For the XR-2207 FSK modulator, set  $R_1 \approx 30 \text{ k}\Omega$ . Now, select a value of  $C_0$  to generate 10.175 kHz with  $R_1$ :
 
$$10.175 \text{ kHz} = 1/(C_0 \times 30,000) ; C_0 = 3300 \text{ pF.}$$

To choose  $R_2$ :

$$18,500 \text{ kHz} - 10.175 \text{ kHz} = 8,325 \text{ kHz} = 1/C_0 R_2 ; R_2 = 36 \text{ k}\Omega.$$

A good choice would be to use 10 k $\Omega$  potentiometers for  $R_{1A}$  and  $R_{2A}$ , and to set  $R_{1B} = 24 \text{ k}\Omega$  and  $R_{2B} = 30 \text{ k}\Omega$ .
- For the XR-2206, we can make  $R_7$  equal to  $R_6$  and  $C_3$  equal to  $C_0$  above. To determine  $R_6$ :
 
$$18.5 \text{ kHz} = 1/R_6 C_3 ; R_6 = 16 \text{ k}\Omega.$$

Use a 10 k $\Omega$  potentiometer for  $R_{6A}$  and set  $R_{6B} = 13 \text{ k}\Omega$ .
  - For the XR-2211 demodulator, we need to first determine  $R_4$  and  $C_1$ . First,  $f_0 = (f_L + f_H)/2 = (10.175 + 18,500)/2 = 14,338 \text{ kHz}$ . If we make  $R_4 = 25 \text{ k}\Omega$ , then  $1/(C_1 \times 25,000) = 14,338$ ;  $C_1 = 2790 \text{ pF} \approx 2700 \text{ pF}$ . With that value of  $C_1$ , the precise value of  $R_4$  is now 25.8 k $\Omega$ . Select  $R_{4B} = 18 \text{ k}\Omega$  and use a 10 k $\Omega$  for  $R_{4A}$ .
  - Frequency Component Selection
    - To calculate  $R_5$ , we first need our  $\Delta f$ , which is  $18,500 - 10.175$ , or 8,325 kHz.
 
$$8325 = (25,800 \times 14,338)/R_5 ; R_5 = 44.4 \text{ k}\Omega \approx 47 \text{ k}\Omega.$$
    - To determine  $C_2$  use  $f = 1/2 = 1/2 \sqrt{C_1/C_2}$ . Then,  $C_2 = 1/2 C_1 ; C_2 = 670 \text{ pF}$ .
    - To select  $C_F$ , we use  $\tau_F = [0.3/(\text{baud rate})]$  seconds.
 
$$\tau_F = 0.3/10,000 = 30 \mu\text{sec. ;}$$

with

$$\tau_F = 100 \text{ k}\Omega, C_F = 300 \text{ pF.}$$

# XR-2211

## FSK Demodulator/Tone Decoder

4. **Lock Range Selection**  
To select  $C_D$ , let us start with the actual lock range:  
 $\Delta f = R_4 f_0 / R_5 = 7870 \text{ Hz}$   
If we assume a capture range of 80%,  
 $\Delta f_c = 6296 \text{ Hz}$   
therefore, our total capture range or  $\pm \Delta f_c$  is 12,592 Hz.  
Our minimum value for  $C_D$  is  $(16/12,592) \mu\text{f}$  or  $0.0013 \mu\text{f}$ .

### 5. Completed Circuit Example

See Figure 5.

- B. **Design a 3 kilobaud modem to operate with low output jitter. The bandwidth available is 13 kHz.**

For this modem, we can take the values from 2 for the 300 baud modem operating at 1070 Hz and 1270 Hz, multiply our baud rate and mark and space frequencies by 10, and divide all capacitor values on the table by 10. Resistor values should be left as they are.

- C. **Design a 2 channel multiplex FSK modulator to operate at the following pairs of mark and space frequencies: 600 Hz and 900 Hz, and 1400 Hz and 1700 Hz. (Each of these channels could handle about 400 baud.)**

For this task, we will use the XR-2207. The only real consideration here is that, if possible, we want to keep the following resistances all between 10 k $\Omega$  and 100 k $\Omega$ :  $R_1$ ,  $R_1/R_2$ ,  $R_3$  and  $R_3/R_4$ . The ratio between the maximum and minimum frequencies is less than 3:1, so we should have no trouble meeting this criterion. If we set our maximum frequency with an R of about 20 k $\Omega$ , we have:  $1700 = 1/(C_0 \times 20,000)$ ;  $C_0 = 0.029 \mu\text{f}$  which is approximately equal to 0.033  $\mu\text{f}$ .

### ADJUSTMENT PROCEDURE

The only adjustments that are required with any of the circuits in this application note are those for frequency fine tuning. Although these adjustments are fairly simple and straightforward, there are a couple of recommendations that should be followed.

**The XR-2207:** Always adjust the lower frequency first with  $R_{1B}$  or  $R_{3B}$  and a low level on pin 9. Then with a high level on pin 9, adjust the high frequency using  $R_{2B}$  or  $R_{4B}$ . The second adjustment affects only the high frequency, whereas the first adjustment affects both the low and the high frequencies.

**The XR-2206:** The upper and lower frequency adjustments are independent so the sequence is not important.

**The XR-2211:** With the input open-circuited, the loop phase detector output voltage is essentially undefined.

Calculating  $R_1$  using 600 Hz and 0.033  $\mu\text{f}$ , we get  $R_1 = 50.5 \text{ k}\Omega$ . We can use  $R_{1B} = 47 \text{ k}\Omega$  and  $R_{1A} = 10 \text{ k}\Omega$ . For  $R_2$ , we get 101 k $\Omega$ . Use  $R_{2B} = 91 \text{ k}\Omega$  and  $R_{2A} = 20 \text{ k}\Omega$ . To determine  $R_3$ , use:  $1400 \text{ Hz} = 1/R_3 C_0$ , which gives us  $R_3 = 21.6 \text{ k}\Omega$ . Use  $R_{3B} = 18 \text{ k}\Omega$  and  $R_{3A} = 5 \text{ k}\Omega$ .  $R_4$  must generate a 300 Hz shift in frequency, the same as  $R_2$ . Therefore set  $R_4$  equal to  $R_2$ .

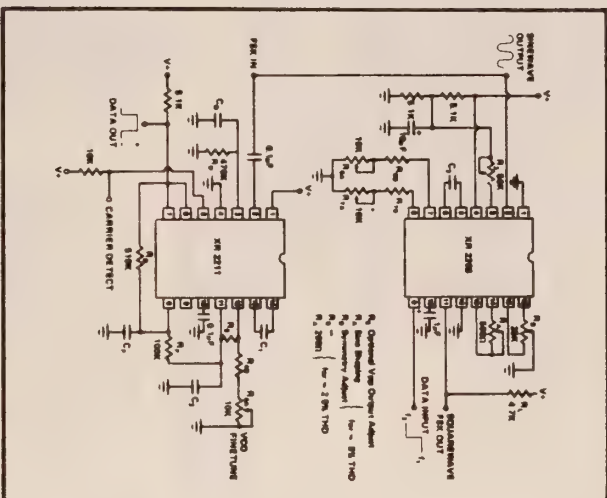


Figure 5. Full Duplex FSK Modem Using XR-2206 and XR-2211. (See Table 2 for Component Values.)

and VCO frequency may be anywhere within the lock range. There are several ways that  $f_0$  can be monitored:

1. Short pin 2 to pin 10 and measure  $f_0$  at pin 3 with  $C_D$  disconnected;
2. Open  $R_3$  and monitor pin 13 or 14 with a high-impedance probe; or
3. Remove the resistor between pins 7 and 8 and find the input frequency at which the FSK output changes state.

**Note:** Do NOT adjust the center frequency of the XR-2211 by monitoring the timing capacitor for frequency with everything connected and no input signal applied.

For further information regarding the use of the XR-2207, XR-2206 and XR-2211 refer to the individual product data sheets.

### FEATURES

- Wide Frequency Range  
0.01 Hz to 300 kHz
- Wide Supply Voltage Range  
4.5V to 20V
- DTL/TTL/ECL Logic Compatibility
- FSK Demodulation, with Carrier-Detection
- Wide Dynamic Range
- Adjustable Tracking Range ( $\pm 1\%$  to  $\pm 80\%$ )
- Excellent Temp. Stability  
20 ppm/ $^{\circ}\text{C}$ , typ.

### APPLICATIONS

- FSK Demodulation
- Data Synchronization
- Tone Decoding
- FM Detection
- Carrier Detection

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL, and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay.

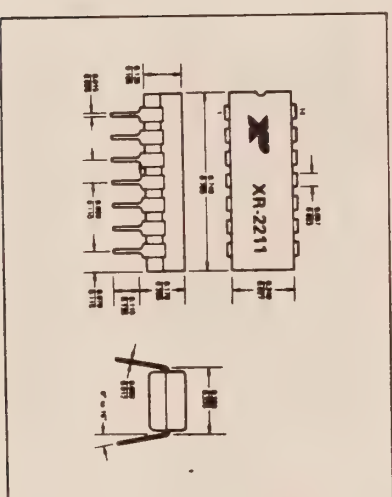
### ABSOLUTE MAXIMUM RATINGS

- Power Supply  
20V
- Input Signal Level  
3V rms
- Power Dissipation  
750 mW
- Ceramic Package:  
Derate above  $T_A = +25^{\circ}\text{C}$   
6 mW/ $^{\circ}\text{C}$
- Plastic Package:  
Derate above  $T_A = +25^{\circ}\text{C}$   
5.0 mW/ $^{\circ}\text{C}$

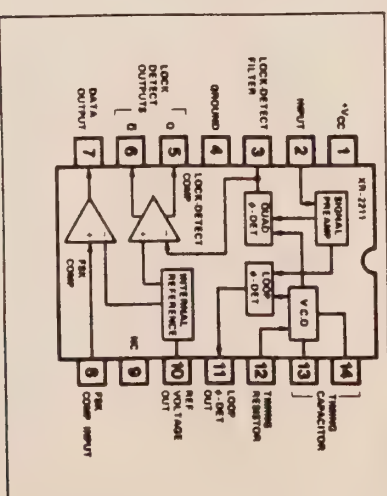
### AVAILABLE TYPES

- | Part Number | Package | Operating Temperature                           |
|-------------|---------|---|
| XR-2211M    | Ceramic | $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ |
| XR-2211CN   | Ceramic | $0^{\circ}\text{C}$ to $+75^{\circ}\text{C}$    |
| XR-2211CP   | Plastic | $0^{\circ}\text{C}$ to $+75^{\circ}\text{C}$    |
| XR-2211N    | Ceramic | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$  |
| XR-2211P    | Plastic | $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$  |

### PACKAGE INFORMATION



### FUNCTIONAL BLOCK DIAGRAM



# **ELECTRICAL CHARACTERISTICS**

Test Conditions:  $V^+ = +12V$ ,  $T_A = +25^\circ C$ ,  $R_0 = 30\text{ K}\Omega$ ,  $C_0 = 0.033\text{ }\mu F$ . See Fig. 2 for component designation

CHARACTERISTICS	XR-2211/2211M		XR-2211C		CONDITIONS
	MIN.	TYP.	MAX.	MAX.	
<b>GENERAL</b>					
Supply Voltage	4.5		20	20	V
Supply Current		4	5	9	mA
<b>OSCILLATOR SECTION</b>					
Frequency Accuracy		$\pm 1$	$\pm 3$		%
Frequency Stability		$\pm 20$	$\pm 50$		ppm/°C
Temperature		0.05	0.5		%/V
Power Supply		0.2	300		%/V
Upper Frequency Limit	100	300			kHz
Lower Frequency Limit			0.01		Hz
Operating Frequency					KHz
Timing Resistor, $R_0$	5		2000	2000	K $\Omega$
Operating Range	15		100	100	K $\Omega$
Recommended Range					
<b>LOOP PHASE DETECTOR SECTION</b>					
Peak Output Current	$\pm 150$	$\pm 200$	$\pm 300$		$\mu A$
Output Offset Current	$\pm 1$	$\pm 1$	$\pm 300$		$\mu A$
Output Impedance	$\pm 4$	$\pm 5$			M $\Omega$
Maximum Swing					V
<b>QUADRATURE PHASE DETECTOR</b>					
Peak Output Current	100	150			$\mu A$
Output Impedance	1	1			M $\Omega$
Maximum Swing					Vpp
<b>INPUT PREAMP SECTION</b>					
Input Impedance		20			K $\Omega$
Input Signal		2			mV rms
Voltage Required to Cause Limiting		10			K $\Omega$
<b>VOLTAGE COMPARATOR SECTIONS</b>					
Input Impedance		2			M $\Omega$
Input Bias Current		100			nA
Voltage Gain	55	70			dB
Output Voltage Low		300			mV
Output Leakage Current		.01			$\mu A$
<b>INTERNAL REFERENCE</b>					
Voltage Level	4.9	5.3	5.7	5.85	V
Output Impedance		100		100	$\Omega$

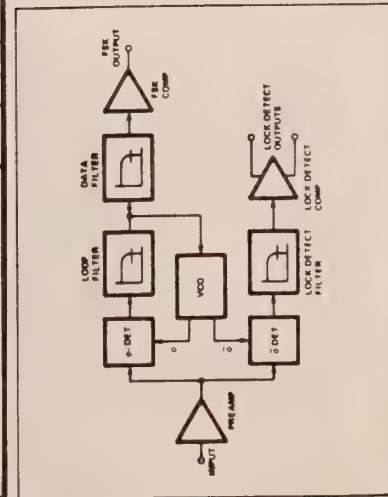


Figure 1. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211.

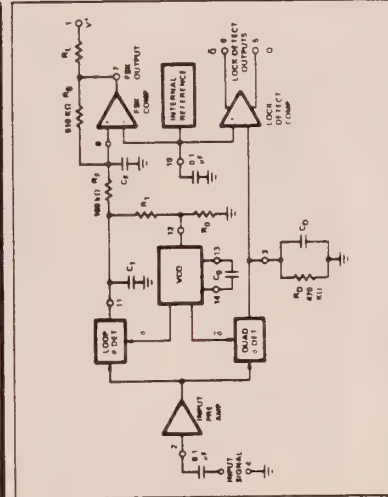


Figure 2. Generalized Circuit Connection for FSK and Tone Detection.

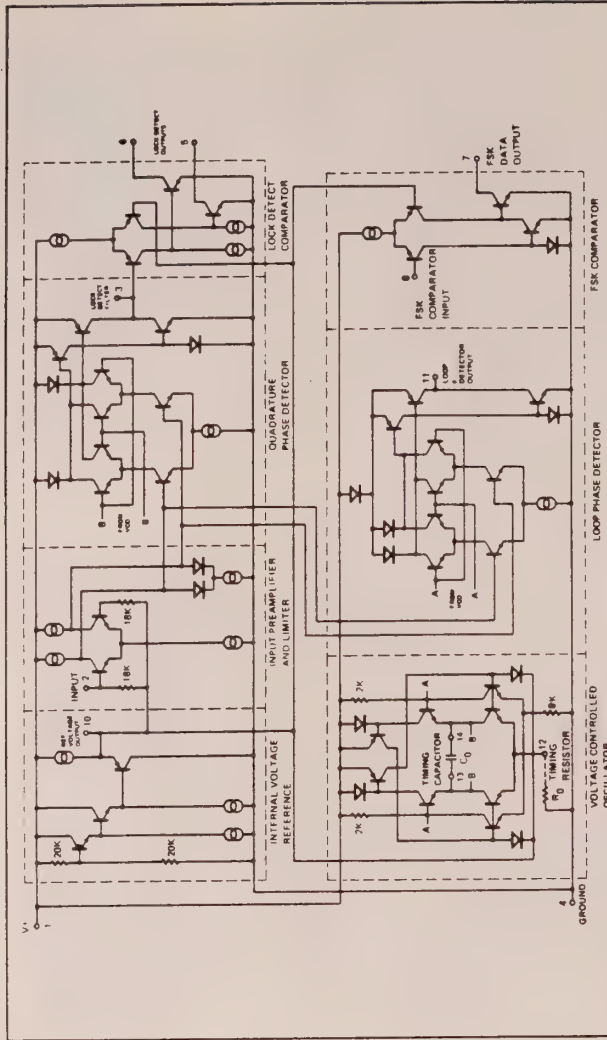


Figure 3. Simplified Circuit Schematic of XR-2211.

## **TYPICAL CHARACTERISTICS**

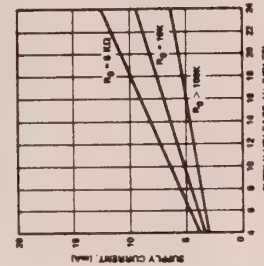


Figure 4. Typical Supply Current vs  $V^+$  (Logic Outputs Open Circuited).

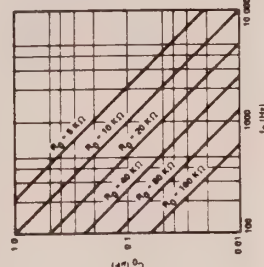


Figure 5. VCO Frequency vs Timing Resistor

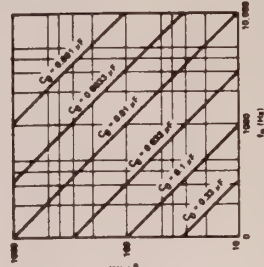


Figure 6. VCO Frequency vs Timing Capacitor

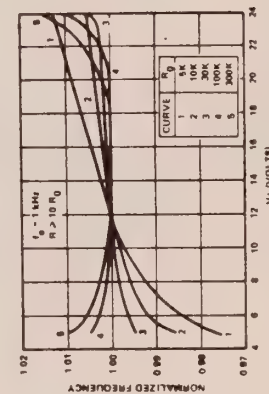


Figure 7. Typical  $f_0$  vs Power Supply Characteristics.

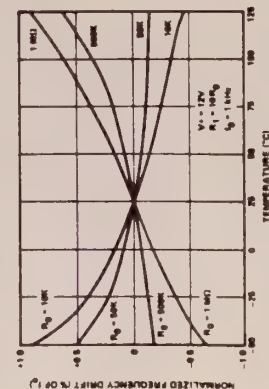


Figure 8. Typical Center Frequency Drift vs Temperature

## DESCRIPTION OF CIRCUIT CONTROLS

**Signal Input (Pin 2):** Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20 K $\Omega$ . Recommended input signal level is in the range of 10 mVrms to 3 Vrms.

**Quadrature Phase Detector Output (Pin 3):** This is the high-impedance output of quadrature phase detector, and is internally connected to the input of lock-detect voltage-comparator. In tone detection applications, Pin 3 is connected to ground through a parallel combination of  $R_D$  and  $C_D$  (See Fig. 2) to eliminate the chatter at lock-detect outputs. If the tone-detect section is not used, Pin 3 can be left open circuited.

**Lock-Detect Output, Q (Pin 5):** The output at Pin 5 is at "high" state when the PLL is out of lock and goes to "low" or conducting state when the PLL is locked. It is an open-collector type output and requires a pull-up resistor,  $R_L$ , to  $V+$  for proper operation. At "low" state, it can sink up to 5 mA of load current.

**Lock-Detect Complement,  $\bar{Q}$  (Pin 6):** The output at Pin 6 is the logic complement of the lock-detect output at Pin 5. This output is also an open-collector type output which can sink 5 mA of load current at low or "on" state.

**FSK Data Output (Pin 7):** This output is an open-collector logic stage which requires a pull-up resistor,  $R_L$ , to  $V+$  for proper operation. It can sink 5 mA of load current. When decoding FSK signals, FSK data output is at "high" or off state for low input frequency, and at "low" or on state for high input frequency. If no input signal is present, the logic state at Pin 7 is indeterminate.

**FSK Comparator Input (Pin 8):** This is the high-impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase-detector output (Pin 11). This data filter is formed by  $R_F$  and  $C_F$  of Fig. 2. The threshold voltage of the comparator is set by the internal reference voltage,  $V_R$ , available at Pin 10.

**Reference Voltage,  $V_R$  (Pin 10):** This pin is internally biased at the reference voltage level,  $V_R$ .  $V_R = V+/2 - 650$  mV. The dc voltage level at this pin forms an internal reference for the voltage levels at pins 5, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1  $\mu$ F capacitor, for proper operation of the circuit.

**Loop Phase Detector Output (Pin 11):** This terminal provides a high-impedance output for the loop phase-detector. The PLL loop filter is formed by  $R_1$  and  $C_1$  connected to Pin 11 (See Fig. 2). With no input signal, or with no phase-error within the PLL, the dc level at Pin 11 is very nearly equal to  $V_R$ . The peak voltage swing available at the phase detector output is equal to  $\pm V_R$ .

**VCO Control Input (Pin 12):** VCO free-running frequency is determined by external timing resistor,  $R_0$ , connected from this terminal to ground. The VCO free-running frequency,  $f_0$ , is:

$$f_0 = \frac{1}{R_0 C_0} \text{ Hz}$$

where  $C_0$  is the timing capacitor across pins 13 and 14. For optimum temperature stability,  $R_0$  must be in the range of 10 K $\Omega$  to 100 K $\Omega$  (See Fig. 8).

This terminal is a low-impedance point, and is internally biased at a dc level equal to  $V_R$ . The maximum timing current drawn from Pin 12 must be limited to  $\leq 3$  mA for proper operation of the circuit.

**VCO Timing Capacitor (Pins 13 and 14):** VCO frequency is inversely proportional to the external timing capacitor,  $C_0$ , connected across these terminals (See Fig. 5).  $C_0$  must be non-polar, and in the range of 200 pF to 10  $\mu$ F.

**VCO Frequency Adjustment:** VCO can be fine-tuned by connecting a potentiometer,  $R_X$ , in series with  $R_0$  at Pin 12 (See Fig. 9).

**VCO Free-Running Frequency,  $f_0$ :** XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase-detector sections of the circuit. However, for set-up or adjustment purposes, VCO free-running frequency can be measured at Pin 3 (with  $C_D$  disconnected), with no input and with Pin 2 shorted to Pin 10.

## DESIGN EQUATIONS

(See Fig. 2 for Definition of Components)

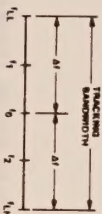
1. VCO Center Frequency,  $f_0$ :  
 $f_0 = 1/R_0 C_0$  Hz

2. Internal Reference Voltage,  $V_R$  (measured at Pin 10)  
 $V_R = V+/2 - 650$  mV

3. Loop Low-Pass Filter Time Constant,  $\tau$ :  
 $\tau = R_1 C_1$

4. Loop Damping,  $\zeta$ :  
 $\zeta = 1/4 \sqrt{C_0/C_1}$

5. Loop Tracking Bandwidth,  $\pm \Delta f/f_0$ :  
 $\Delta f/f_0 = R_0/R_1$



6. FSK Data Filter Time Constant,  $\tau_F$ :  
 $\tau_F = R_F C_F$

7. Loop Phase Detector Conversion Gain,  $K_\phi$ : ( $K_\phi$  is the differential dc voltage across Pins 10 and 11, per unit of phase error at phase-detector input)  
 $K_\phi = -2V_R/\pi$  volts/radian

8. VCO Conversion Gain,  $K_0$ : ( $K_0$  is the amount of change in VCO frequency, per unit of dc voltage change at Pin 12):  
 $K_0 = -1/V_R C_0 R_1$  Hz/volt

9. Total Loop Gain,  $K_T$ :  
 $K_T = 2\pi K_\phi K_0 = 4/C_0 R_1$  rad/sec/volt

10. Peak Phase-Detector Current,  $I_A$ :  
 $I_A = V_R$  (volts)/25 mA

## APPLICATIONS INFORMATION

### FSK DECODING:

Figure 9 shows the basic circuit connection for FSK decoding. With reference to Figures 2 and 9, the functions of external components are defined as follows:  $R_0$  and  $C_0$  set the PLL center frequency,  $R_1$  sets the system bandwidth, and  $C_1$  sets the loop filter time constant and the loop damping factor.  $C_F$  and  $R_F$  form a one-pole post-detection filter for the FSK data output. The resistor  $R_D$  (510 K $\Omega$ ) from Pin 7 to Pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states. Recommended component values for some of the most commonly used FSK bands are given in Table I.

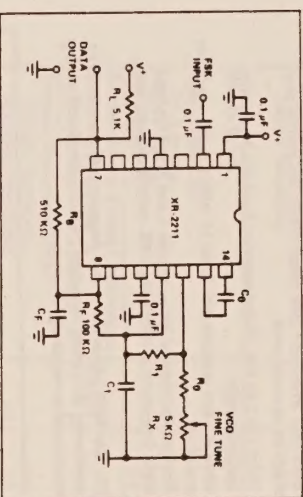


Figure 9. Circuit Connection for FSK Decoding

### Design Instructions:

The circuit of Fig. 9 can be tailored for any FSK decoding application by the choice of five key circuit components:  $R_0$ ,  $R_1$ ,  $C_0$ ,  $C_1$  and  $C_F$ . For a given set of FSK mark and space frequencies,  $f_1$  and  $f_2$ , these parameters can be calculated as follows:

$$f_0 = \frac{f_1 + f_2}{2}$$

- a) Calculate PLL center frequency,  $f_0$ :
- b) Choose value of timing resistor  $R_0$ , to be in the range of 10 K $\Omega$  to 100 K $\Omega$ . This choice is arbitrary. The recommended value is  $R_0 \approx 20$  K $\Omega$ . The final value of  $R_0$  is normally fine-tuned with the series potentiometer,  $R_X$ .
- c) Calculate value of  $C_0$  from design equation (1) or from Fig. 6:

- d) Calculate  $R_1$  to give a  $\Delta f$  equal to the mark-space deviation:

$$R_1 = R_0 [f_0/(f_1 - f_2)]$$

- e) Calculate  $C_1$  to set loop damping. (See Design Equation No. 4).  
Normally,  $\zeta \approx 1/2$  is recommended.

- f) Calculate Data Filter Capacitance,  $C_F$ :  
For  $R_F = 100$  K $\Omega$ ,  $R_D = 510$  K $\Omega$ , the recommended value of  $C_F$  is:

$$C_F \approx 3/(\text{Baud Rate}) \mu\text{F}$$

Note: All calculated component values except  $R_0$  can be rounded-off to the nearest standard value, and  $R_0$  can be varied to fine-tune center frequency, through a series potentiometer,  $R_X$ . (See Fig. 9).

### Design Example:

75 Baud FSK demodulator with mark/space frequencies of 1110/1170 Hz:

- Step 1: Calculate  $f_0 = (1110 + 1170)/(1/2) = 1140$  Hz
  - Step 2: Choose  $R_0 = 20$  K $\Omega$  (18 K $\Omega$  fixed resistor in series with 5 K $\Omega$  potentiometer)
  - Step 3: Calculate  $C_0$  from Fig. 6:  $C_0 = 0.044 \mu\text{F}$
  - Step 4: Calculate  $R_1$ :  $R_1 = R_0(2240/60) = 380$  K $\Omega$
  - Step 5: Calculate  $C_1$ :  $C_1 = C_0/4 = 0.011 \mu\text{F}$
- Note: All values except  $R_0$  can be rounded-off to nearest standard value.

FSK BAND	COMPONENT VALUES
300 Baud $f_1 = 1070$ Hz $f_2 = 1270$ Hz	$C_0 = 0.039 \mu\text{F}$ $C_F = 0.005 \mu\text{F}$ $C_1 = 0.01 \mu\text{F}$ $R_0 = 18$ K $\Omega$ $R_1 = 100$ K $\Omega$
300 Baud $f_1 = 2025$ Hz $f_2 = 2225$ Hz	$C_0 = 0.022 \mu\text{F}$ $C_F = 0.005 \mu\text{F}$ $C_1 = 0.0047 \mu\text{F}$ $R_0 = 18$ K $\Omega$ $R_1 = 200$ K $\Omega$
1200 Baud $f_1 = 1200$ Hz $f_2 = 2200$ Hz	$C_0 = 0.027 \mu\text{F}$ $C_F = 0.0022 \mu\text{F}$ $C_1 = 0.01 \mu\text{F}$ $R_0 = 18$ K $\Omega$ $R_1 = 30$ K $\Omega$

TABLE I

Recommended Component Values for Commonly Used FSK Bands (See Circuit of Fig. 9)

### FSK DECODING WITH CARRIER-DETECT:

The lock-detect section of XR-2211 can be used as a carrier-detect option, for FSK decoding. The recommended circuit connection for this application is shown in Fig. 10. The open-collector lock-detect output, Pin 6, is shorted to data output (Pin 7). Thus, data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL, and the Pin 6 output goes "high", to enable the data output.

The minimum value of the lock-detect filter capacitance  $C_D$  is inversely proportional to the capture range,  $\pm \Delta f_c$ . This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by  $C_1$ . For most applications,  $\Delta f_c > \Delta f/2$ . For  $R_D = 470$  K $\Omega$ , the approximate minimum value of  $C_D$  can be determined by:

$$C_D (\mu\text{F}) \geq 16/\text{capture range in Hz.}$$

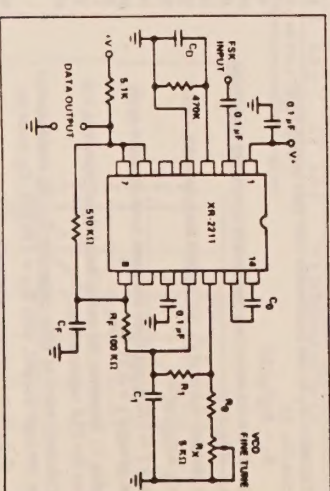


Figure 10. External Connectors for FSK Demodulation with Carrier-Detect Capability.  
Note: Data Output is "Low" When No Carrier is Present.

With values of  $C_D$  that are too small, chatter can be observed on the lock-detect output as an incoming signal frequency approaches the capture bandwidth. Excessively-large values of  $C_D$  will slow the response time of the lock-detect output.

#### TONE DETECTION:

Figure 11 shows the generalized circuit connection for tone detection. The logic outputs, Q and  $\bar{Q}$  at Pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5 mA of load current.

Both logic outputs at Pins 5 and 6 are open-collector type stages, and require external pull-up resistors  $R_{L1}$  and  $R_{L2}$ , as shown in Fig. 11.

With reference to Figs. 2 and 11, the functions of the external circuit components can be explained as follows:  $R_0$  and  $C_0$  set VCO center frequency;  $R_1$  sets the detection bandwidth;  $C_1$  sets the low pass-loop filter time constant and the loop damping factor.  $R_{L1}$  and  $R_{L2}$  are the respective pull-up resistors for the Q and  $\bar{Q}$  logic outputs.

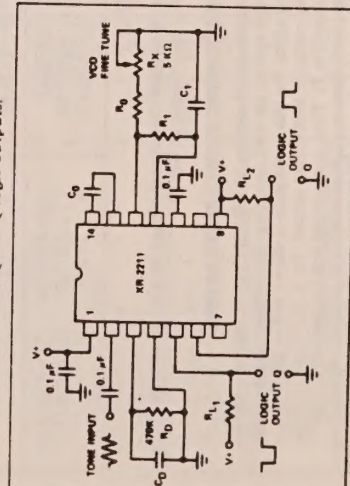


Figure 11. Circuit Connection for Tone Detection

#### Design Instructions:

The circuit of Fig. 11 can be optimized for any tone-detection application by the choice of the 5 key circuit components:  $R_0$ ,  $R_1$ ,  $C_0$ ,  $C_1$  and  $C_D$ . For a given input tone frequency,  $f_S$ , these parameters are calculated as follows:

- Choose  $R_0$  to be in the range of 15 K $\Omega$  to 100 K $\Omega$ . This choice is arbitrary.
- Calculate  $C_0$  to set center frequency,  $f_0$  equal to  $f_S$ : (See Fig. 6).  $C_0 = 1/R_0 f_S$
- Calculate  $R_1$  to set bandwidth  $\pm \Delta f$ : (see design Equation No. 5):  
 $R_1 = R_0 f_0 / \Delta f$

Note: The total detection bandwidth covers the frequency range of  $f_0 \pm \Delta f$ .

- Calculate value of  $C_1$  for a given loop damping factor:  
 $C_1 = C_0 / 16 f_S^2$

Normally  $f \approx 1/2$  is optimum for most tone-detector applications, giving  $C_1 = 0.25 C_0$ .

Increasing  $C_1$  improves the out-of-band signal rejection, but increases the PLL capture time.

- Calculate value of filter capacitor  $C_D$ . To avoid chatter at the logic output, with  $R_D = 470$  K $\Omega$ ,  $C_D$  must be:  
 $C_D (\mu F) \geq (16 / \text{capture range in Hz})$

Increasing  $C_D$  slows down the logic output response time.

#### Design Examples:

Tone detector with a detection band of 1 kHz  $\pm$  20 Hz:

- Choose  $R_0 = 20$  K $\Omega$  (18 K $\Omega$  in series with 5 K $\Omega$  potentiometer).
- Choose  $C_0$  for  $f_0 = 1$  kHz: From Fig. 6:  $C_0 = 0.05 \mu F$ .
- Calculate  $R_1$ :  $R_1 = (R_0) (1000/20) = 1$  M $\Omega$ .
- Calculate  $C_1$ : for  $f = 1/2$ ,  $C_1 = 0.25$ ,  $C_0 = 0.013 \mu F$ .
- Calculate  $C_D$ :  $C_D = 16/38 = 0.42 \mu F$ .
- Fine-tune center frequency with 5 K $\Omega$  potentiometer,  $R_X$ .

#### ADJUSTMENT PROCEDURE

With the input open-circuited, the loop phase detector output voltage is essentially undefined and VCO frequency may be anywhere within the lock range. There are several ways that  $f_0$  can be monitored:

- Short pin 2 to pin 10 and measure  $f_0$  at pin 3 with  $C_D$  disconnected;
- Open  $R_1$  and monitor pin 13 or 14 with a high-impedance probe; or
- Remove the resistor between pins 7 and 8 and find the input frequency at which the FSK output changes state.

NOTE: Do NOT adjust the center frequency of the XR-2211 by monitoring the timing capacitor frequency with everything connected and no input signal applied.

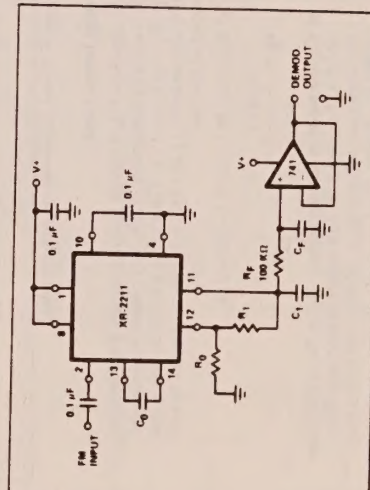


Figure 12. Linear FM Detector Using XR-2211 and an External Op. Amp. (See section on Design Equations, for Component Values)

#### LINEAR FM DETECTION:

XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this application is shown in Fig. 12. The demodulated output is taken from the loop phase detector output (Pin 11), through a post detection filter made up of  $R_F$  and  $C_F$ , and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at Pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Fig. 12.

The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

$$V_{out} = R_1 V_R / 100 R_0 \text{ Volts}/\% \text{ deviation}$$

where  $V_R$  is the internal reference voltage. ( $V_R = V_{+}/2 - 650$  mV). For the choice of external components  $R_1$ ,  $R_0$ ,  $C_D$ ,  $C_1$  and  $C_F$ , see section on Design Equations.

Remember:  
STATION NODS  
145.65 MHz  
POINT to POINT &  
RAC CHSW  
146.46 MHz

# XR-2206

## Monolithic Function Generator

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp and pulse waveforms of high stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01 Hz to more than 1 MHz.

The XR-2206 is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM or FSK generation. It has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage with very little effect on distortion.

As shown in Figure 1, the monolithic circuit is comprised of four functional blocks: a voltage-controlled oscillator (VCO); an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches. The internal current switches transfer the oscillator current to any one of the two external timing resistors to produce two discrete frequencies selected by the logic level at the FSK input terminal (pin 9).

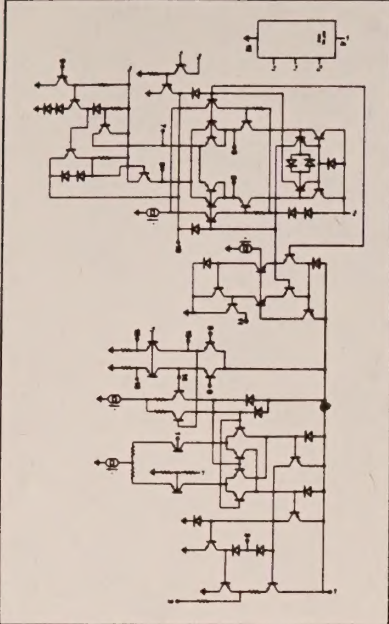
### FEATURES

- Low Sinewave Distortion (THD, 5%) – insensitive to signal sweep
- Excellent Stability (20 ppm/°C, typ)
- Wide Sweep Range (2000:1, typ)
- Low Supply Sensitivity (0.01%/V, typ)
- Linear Amplitude Modulation
- Adjustable Duty-Cycle (1% to 99%)
- TTL Compatible FSK Controls
- Wide Supply Range (10V to 26V)

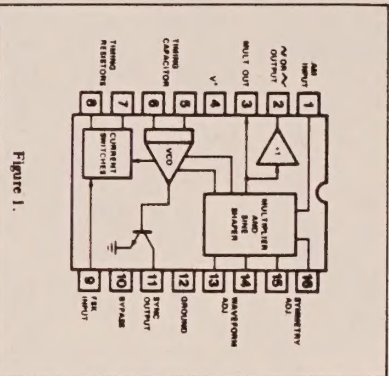
### APPLICATIONS

- Waveform Generation  
Sine, Square, Triangle, Ramp
- Sweep Generation
- AM/FM Generation
- FSK and PSK Generation
- Voltage-to-Frequency Conversion
- Tone Generation
- Phase-Locked Loops

### EQUIVALENT SCHEMATIC DIAGRAM



### FUNCTIONAL BLOCK DIAGRAM



### ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of Fig. 2,  $V^+ = 12V$ ,  $T_A = 25^\circ C$ ,  $C = 0.01 \mu F$ ,  $R_1 = 100 K\Omega$ ,  $R_2 = 10 K\Omega$ ,  $R_3 = 25 K\Omega$  unless otherwise specified. S1, open for triangle, closed for sine wave.

CHARACTERISTICS	XR-2206/XR-2206M			XR-2206C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
Supply Voltage	10		26	10		26	V	
Single Supply	$\pm 5$		$\pm 13$	$\pm 5$		$\pm 13$	V	
Supply Current	12		17	14		20	mA	$R_1 \geq 10 K\Omega$
Oscillator Section								
Max. Operating Frequency	0.5	1	0.5	1			MHz	$C = 1000 pF$ , $R_1 = 1 K\Omega$
Lowest Practical Frequency	0.01	0.01	0.01	0.01			Hz	$C = 50 \mu F$ , $R_1 = 2 M\Omega$
Frequency Accuracy	$\pm 1$	$\pm 4$	$\pm 4$	$\pm 2$			% of $f_0$	$f_0 = 1/R_1 C$
Temperature Stability	$\pm 10$	$\pm 50$	$\pm 50$	$\pm 20$			ppm/°C	$0^\circ C \leq T_A \leq 75^\circ C$ , $R_1 = R_2 = 20 K\Omega$
Supply Sensitivity	0.01	0.1	0.1	0.01			%/V	$V_{LOW} = 10V$ , $V_{HIGH} = 20V$ , $R_1 = R_2 = 20 K\Omega$
Sweep Range	1000:1	2000:1		2000:1				
Sweep Linearity							$f_H = f_L$	$f_H @ R_1 = 1 K\Omega$
10:1 Sweep		2		2			%	$f_L @ R_1 = 2 M\Omega$
1000:1 Sweep		8		8			%	$f_L = 1 kHz$ , $f_H = 10 kHz$
FM Distortion		0.1		0.1			%	$f_L = 100 Hz$ , $f_H = 100 kHz$
Recommended Timing Components								$\pm 10\%$ Deviation
Timing Capacitor: C							$\mu F$	See Figure 5
Timing Resistors: $R_1$ & $R_2$	0.001		100	0.001		100	K $\Omega$	See Figure 5
Triangle/Sinewave Output								
Triangle Amplitude		160	80	160			mV/K $\Omega$	See Note 1, Fig. 3
Sinewave Amplitude	40	60	60	60			mV/K $\Omega$	Fig. 2 S1 Open
Max. Output Swing		6	6	6			Vpp	Fig. 2 S1 Closed
Output Impedance		600	1	600			$\Omega$	
Triangle Linearity		1	0.5	1			%	
Amplitude Stability		0.5		0.5			dB	
Sinewave Amplitude Stability		-4800		-4800			ppm/°C	For 1000:1 Sweep
Sinewave Distortion								See Note 2
Without Adjustment		2.5	1.0	2.5		1.5	%	$R_1 = 30 K\Omega$
With Adjustment		0.4		0.5			%	See Figure 11
Amplitude Modulation								See Figure 12
Input Impedance	50	100	50	100			K $\Omega$	
Modulation Range		100		100			%	
Carrier Suppression		55		55			dB	
Linearity		2		2				
Square Wave Output								For 95% modulation
Amplitude		12		12			Vpp	Measured at Pin 11
Rise Time		250		250			nsec	$C_L = 10 pF$
Fall Time		50		50			nsec	$C_L = 10 pF$
Saturation Voltage		0.2	0.4	0.6			V	$I_L = 2 mA$
Leakage Current		0.1	20	100			$\mu A$	$V_{II} = 26V$
FSK Keying Level (Pin 9)	0.8	1.4	2.4	0.8	1.4	2.4	V	See Section on Circuit Controls
Reference Bypass Voltage	2.9	3.1	3.3	2.5	3	3.5	V	Measured at Pin 10.

Note 1: Output amplitude is directly proportional to the resistance  $R_3$  on Pin 3. See Figure 3.

Note 2: For maximum amplitude stability  $R_3$  should be a positive temperature coefficient resistor.

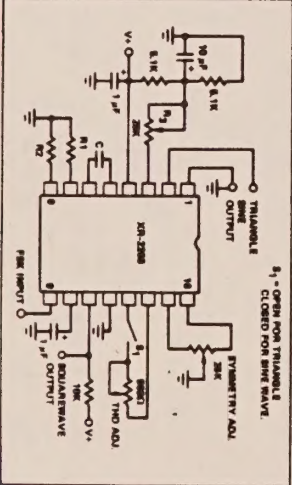


Figure 2. Basic Test Circuit

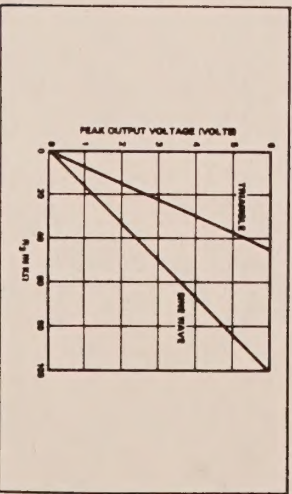


Figure 3. Output Amplitude as a Function of Resistor  $R_3$  at Pin 3.

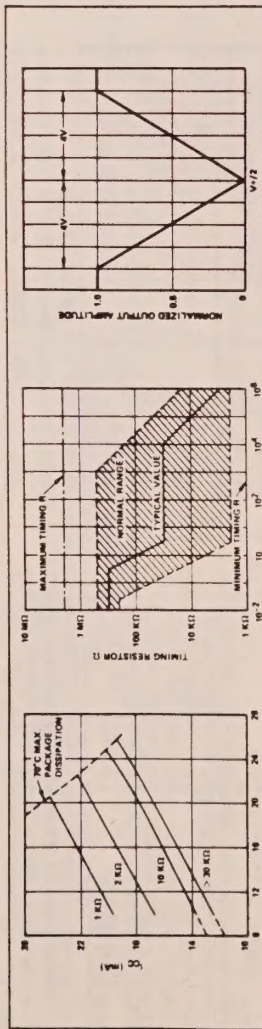


Figure 4. Supply Current vs Supply Voltage, Timing R

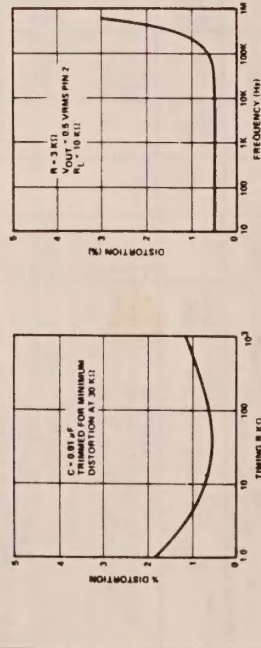


Figure 5. R vs Oscillation Frequency

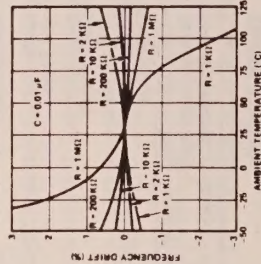


Figure 6. Normalized Output Amplitude vs DC Bias at AM Input (Pin 1).

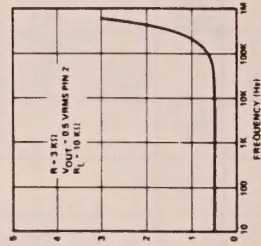


Figure 7. Trimmed Distortion vs Timing Resistor

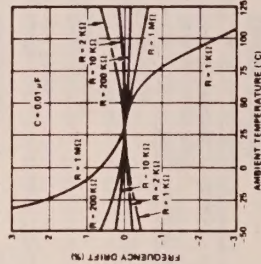


Figure 8. Signwave Distortion vs Operating Frequency With Timing Capacitors Varied

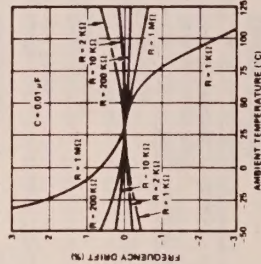


Figure 9. Frequency Drift vs Temperature

## DESCRIPTION OF CIRCUIT CONTROLS

### FREQUENCY OF OPERATION:

The frequency of oscillation,  $f_o$ , is determined by the external timing capacitor C across pins 5 and 6, and by the timing resistor R connected to either pin 7 or pin 8. The frequency is given as

$$f_o = \frac{1}{RC} \text{ Hz}$$

and can be adjusted by varying either R or C. The recommended values of R for a given frequency range are shown in Figure 5. Temperature stability is optimum for  $4 \text{ K}\Omega < R < 200 \text{ K}\Omega$ . Recommended values of C are from  $1000 \text{ pF}$  to  $100 \mu\text{F}$ .

### FREQUENCY SWEEP AND MODULATION

Frequency of oscillation is proportional to the total timing current  $I_T$  drawn from pin 7 or 8

$$f = \frac{320 I_T (\text{mA})}{C (\mu\text{F})} \text{ Hz}$$

Timing terminals (pins 7 or 8) are low impedance points and are internally biased at  $+3\text{V}$ , with respect to pin 12. Frequency varies linearly with  $I_T$  over a wide range of current values, from  $1 \mu\text{A}$  to  $3 \text{ mA}$ . The frequency can be controlled by applying a control voltage,  $V_C$ , to the activated timing pin as shown in Figure 10. The frequency of oscillation is related to  $V_C$  as:

$$f = \frac{1}{RC} \left[ 1 + \frac{R}{RC} \left( 1 - \frac{V_C}{3} \right) \right] \text{ Hz}$$

where  $V_C$  is in volts. The voltage-to-frequency conversion gain, K, is given as:

$$K = \frac{\partial f / \partial V_C}{f} = - \frac{0.32}{RC} \text{ Hz/V}$$

NOTE: For safe operation of the circuit  $I_T$  should be limited to  $\leq 3 \text{ mA}$ .

resistor is activated. If pin 9 is open-circuited or connected to a bias voltage  $> 2\text{V}$ , only  $R_1$  is active. Similarly, if the voltage level at pin 9 is  $\leq 1\text{V}$ , only  $R_2$  is activated. Thus, the output frequency can be keyed between two levels,  $f_1$  and  $f_2$  as:

$$f_1 = 1/R_1 C \text{ and } f_2 = 1/R_2 C$$

For split-supply operation, the keying voltage at pin 9 is referenced to  $V^-$ .

### OUTPUT DC LEVEL CONTROL

The dc level at the output (pin 2) is approximately the same as the dc bias at pin 3. In Figures 11, 12 and 13, pin 3 is biased mid-way between  $V^+$  and ground, to give an output dc level of  $\approx V^+/2$ .

## APPLICATIONS INFORMATION

### SINEWAVE GENERATION

#### A) Without External Adjustment

Figure 11 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer  $R_1$  at pin 7 provides the desired frequency tuning. The maximum output swing is greater than  $V^+/2$  and the

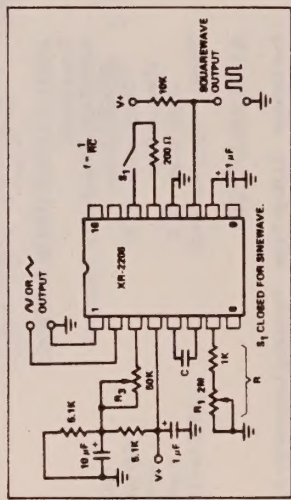


Figure 11. Circuit for Sinewave Generation Without External Adjustment. (See Fig. 3 for choice of  $R_3$ )

typical distortion (THD) is  $< 2.5\%$ . If lower sinewave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of Figure 11 can be converted to split supply operation simply by replacing all ground connections with  $V^-$ . For split supply operation,  $R_3$  can be directly connected to ground.

#### B) With External Adjustment

The harmonic content of sinusoidal output can be reduced to  $\approx 0.5\%$  by additional adjustments as shown in Figure 12. The potentiometer  $R_A$  adjusts the sine-shaping resistor;

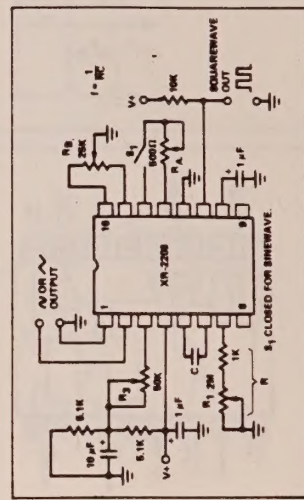


Figure 12. Circuit for Sinewave Generation With Minimum Harmonic Distortion. ( $R_3$  Determines output Swing - See Fig. 3)

and  $R_B$  provides the fine-adjustment for the waveform symmetry. The adjustment procedure is as follows:

1. Set  $R_B$  at mid-point and adjust  $R_A$  for minimum distortion.
2. With  $R_A$  set as above, adjust  $R_B$  to further reduce distortion.

### TRIANGLE WAVE GENERATION

The circuits of Figures 11 and 12 can be converted to triangle wave generation by simply open circuiting pins 13 and 14 (i.e., S1 open). Amplitude of the triangle is approximately twice the sinewave output.

### FSK GENERATION

Figure 13 shows the circuit connection for sinusoidal FSK signal generation. Mark and space frequencies can be independently adjusted by the choice of timing resistors  $R_1$  and  $R_2$ ; and the output is phase-continuous during transitions. The keying signal is applied to pin 9. The circuit can be converted to split-supply operation by simply replacing ground with  $V^-$ .

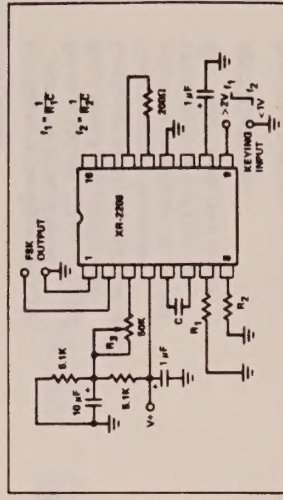


Figure 13. Sinusoidal FSK Generator

### PULSE AND RAMP GENERATION

Figure 14 shows the circuit for pulse and ramp waveform generation. In this mode of operation, the FSK keying terminal (pin 9) is shorted to the square-wave output (pin 11); and the circuit automatically frequency-shift keys itself between two separate frequencies during the positive and negative going output waveforms. The pulse-width and the duty cycle can be adjusted from 1% to 99% by the choice of  $R_1$  and  $R_2$ . The values of  $R_1$  and  $R_2$  should be in the range of  $1 \text{ K}\Omega$  to  $2 \text{ M}\Omega$ .

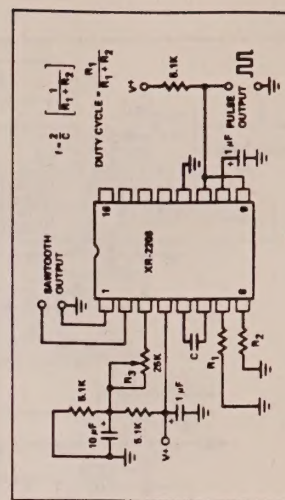


Figure 14. Circuit for Pulse and Ramp Generation